FUJITSU SEMICONDUCTOR
DATA SHEET

DS07-16806-1E

32-bit Microcontroller

CMOS

FR60Lite MB91220/S Series

MB91F223/F223S/MB91V220

■ OVERVIEW

MB91220/S series is a line of single-chip microcontrollers based on a 32-bit high-performance RISC CPU and integrating a variety of I/O resources for embedded control applications.

The MB91220/S series is designed to be best suited for embedded applications which require high-speed and high-performance processing power in the CPU, such as DVD players, printers, TV sets, and the PDP control.The MB91220/S series is a line of CPUs in the FR60Lite implemented by FR* family.

* : FR, the abbreviation of FUJITSU RISC controller, is a line of products of FUJITSU Limited.

Be sure to refer to the “Check Sheet” for the latest cautions on development.

“Check Sheet” is seen at the following support page
URL : http://www.fujitsu.com/global/services/microelectronics/product/micom/support/index.html

“Check Sheet” lists the minimal requirement items to be checked to prevent problems beforehand in system development.

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■ FEATURES

• **FR60Lite CPU**
- 32-bit RISC, load/store architecture, 5-stage pipeline
- Maximum operating frequency : 32 MHz (Source oscillation is 4 MHz with x8 multiplier-PLL clock multiplier system)
- 16-bit fixed-length instructions (basic instructions)
- Instruction execution speed : 1 instruction per cycle
- Instruction set optimized for embedded application : Memory-to-memory transfer, bit manipulation, barrel shift instructions etc.
- Instructions supported by C language : Function entry/exit instructions, multiple-register load/store instructions.
- Register interlock function : Easier assembler coding enabled
- Built-in multiplier supported at the instruction level
  Signed 32-bit multiplication : 5 cycles
  Signed 16-bit multiplication : 3 cycles
- Interrupt (PC/PS save) : 6 cycles (16 priority levels)
- Harvard architecture allowing program access and data access to be executed simultaneously.
- Instruction set compatible with FR family

• **Internal Peripheral Functions**
- Internal ROM size & ROM type
  Flash Memory : 512 Kbytes (MB91F223/S)
- Internal RAM size : 16 Kbytes (MB91F223/S) / 64 Kbytes (MB91V220)
- General-purpose ports : up to 120 ports (including 4 input-only ports)
- 8/10-bit A/D converter (Sequential comparison type)
  8/10-bit resolution : 24 channels
  Conversion time : 3 μs (16/32 MHz)
  Set the PLL multiplier and the division ratio of peripheral circuit clocks so that the above conversion time is achieved.
  32 MHz : Source oscillation (4 MHz) with ×8 multiplier, divided by 1
  16 MHz : Source oscillation with ×8 multiplier, divided by 2
- D/A converter (R-2R type)
  8-bit resolution : 2 channels
- External interrupt : 8 channels
- Bit search module (for REALOS)
- LIN-UART (full duplex double buffer type) : 4 channels
  Synchronous/asynchronous clock operations selectable
  Sync-break detection
  Dedicated built-in baud-rate generator
- I^2C Bus interface* : 2 channels
- Stepping motor controller (SMC) : 4 channels
  10-bit PWM with 4 high-current outputs for each channel
- 8/16-bit PPG timer : 16 channels
- 16-bit reload timer : 3 channels
- 16-bit free-run timer : 2 channels (ICU/OCU linkage)
- 16-bit pulse width counter : 1 channel
- Input capture : 4 channels (free-run timers ch.0 and ch.1). ch.0 linked to PWC
- Output compare : 2 channels (free-run timer ch.0)
- LCD controller : SEG0 to SEG31/COM0 to COM3 (shared with port)
- 16-bit timebase/watch dog timer

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- Sound generator : 3 channels
- Real-time clock
- 32 kHz sub clock (not supported in devices with an S suffix in the part number)
- C-CAN : 2 channels
- Low power consumption modes : sleep mode, stop mode, watch mode
- Package : LQFP-144 (FPT-144P-M08)
- CMOS technology : 0.35 µm
- Power supply voltage : 5 V (Internal logic : 3.3 V, I/O : 5.0 V (step-down circuit used))

* : Purchase of Fujitsu I²C components conveys a license under the Philips I²C Patent Rights to use, these components in an I²C system provided that the system conforms to the I²C Standard Specification as defined by Philips.

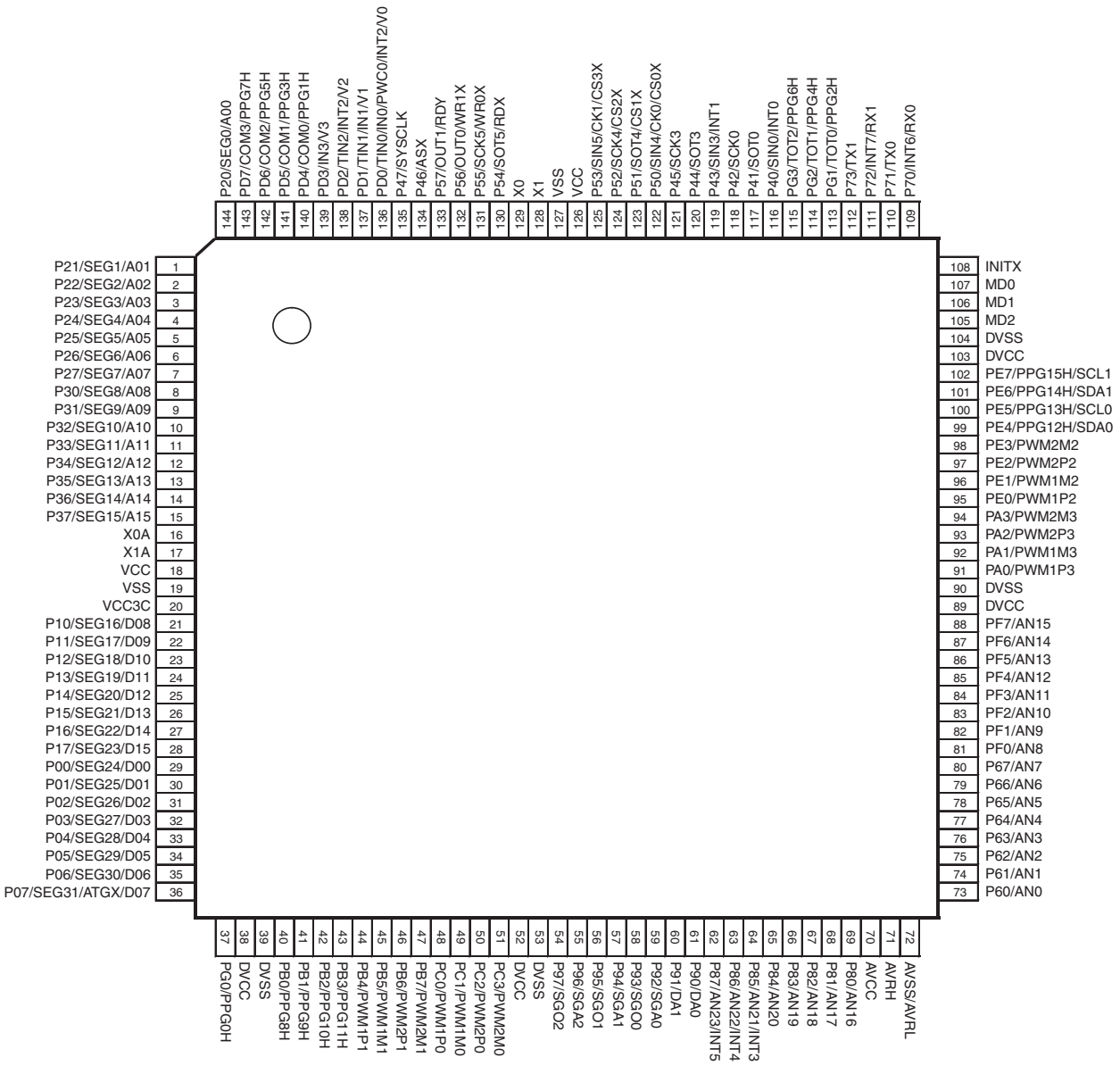
■ PRODUCT LINEUP

The table below shows the product lineup of the MB91220/S series. Embedded peripheral functions which are not listed are common functions.

	MB91V220	MB91F223/S
ROM/Flash size	External SRAM	512 Kbytes
RAM size	64 Kbytes	16 Kbytes
External interrupt	8 channels	
DMA Controller	5 channels	
8 /10-bit A/D Converter	24 channels	
D/A Converter	2 channels	
LIN-UART	4 channels	
I^2C	2 channels	
Stepping Motor Controller	4 channels	
8 /16-bit PPG Timer	16 channels	
16-bit Reload Timer	3 channels	
16-bit Free-Run Timer	2 channels	
16-bit Pulse Width Counter	1 channel	
Input Capture Unit	4 channels	
Output Compare Unit	2 channels	
LCD Controller	4 COM, 32 SEG	
Sound Generator	3 channels	
Real Time Clock	Yes	
32 kHz Sub Clock	Yes	Yes : MB91F223 No : MB91F223S
External bus	Addr 16 bits Data 16 bits	
Others	Evaluation product	Flash memory product
On Chip Debug Support Unit	DSU4	—
C-CAN	2 channels 32-message buffer	

■ PIN ASSIGNMENT

(TOP VIEW)



(FPT-144P-M08)

■ PIN DESCRIPTIONS

Pin No.	Pin name	I/O circuit type*	Function
129	X0	A	Main clock (oscillator) input.
128	X1	A	Main clock (oscillator) output.
16	X0A	B	Sub clock (oscillator) input.
17	X1A	B	Sub clock (oscillator) output.
108	INITX	C	External reset input
105	MD2	D	Mode pin 2. The setting on this pin determines the basic operation mode. Connect it to VCC or VSS.
106	MD1	D	Mode pin 1. The setting on this pin determines the basic operation mode. Connect it to VCC or VSS.
107	MD0	D	Mode pin 0. The setting on this pin determines the basic operation mode. Connect it to VCC or VSS.
29 to 35	P00 to P06	G	General-purpose I/O port
	SEG24 to SEG30		SEG output from LCDC
	D00 to D06		External data bus bit00 to bit06
36	P07	G	General-purpose I/O port
	SEG31		SEG output from LCDC
	ATGX		External trigger input for A/D converter.
	D07		External data bus bit07
21 to 28	P10 to P17	G	General-purpose I/O port
	SEG16 to SEG23		SEG outputs from LCDC
	D08 to D15		External data bus bit08 to bit15
144	P20	F	General-purpose I/O port
	SEG0		SEG output from LCDC
	A00		External address bus bit00
1 to 7	P21 to P27	F	General-purpose I/O port
	SEG1 to SEG7		SEG outputs from LCDC
	A01 to A07		External address bus bit01 to bit07
8 to 15	P30 to P37	F	General-purpose I/O port
	SEG8 to SEG15		SEG outputs from LCDC
	A08 to A15		External address bus bit08 to bit15
116	P40	M	General-purpose I/O port: Valid when the data input specification is prohibited on UART0.
	SIN0		UART0 data input. Because this input is used as necessary while UART0 is used for input operation, the port output needs to be disabled except when it is used intentionally.
	INT0		External interrupt input. Because those inputs are used as necessary while the pertinent external interrupt is enabled, the port outputs need to be disabled except when they are used intentionally.

(Continued)

Pin No.	Pin name	I/O circuit type*	Function
117	P41	I	General-purpose I/O port: Valid when the data output specification is prohibited on UART0.
	SOT0		UART0 data output: Valid when the clock output specification is permitted on UART0 .
118	P42	I	General-purpose I/O port: Valid when the clock output specification is prohibited on UART0.
	SCK0		UART0 clock input/output: Valid when the clock output specification is permitted on UART0.
119	P43	M	General-purpose I/O port: Valid when the data input specification is prohibited on LIN-UART1.
	SIN3		UART1 data input. Because this input is used as necessary while UART1 is used for input operation, the port output needs to be disabled except when it is used intentionally.
	INT1		External interrupt input. Because those inputs are used as necessary while the pertinent external interrupt is enabled, the port outputs need to be disabled except when they are used intentionally.
120	P44	I	General-purpose I/O port: Valid when the data output specification on UART1 is prohibited.
	SOT3		LIN-UART1 data output: Valid when the data output specification is permitted on LIN-UART1.
121	P45	I	General-purpose I/O port: Valid when the clock output specification is prohibited on LIN-UART1.
	SCK3		LIN-UART1 clock input/output: Valid when the clock output specification is permitted on LIN-UART1.
134	P46	I	General-purpose I/O port
	ASX		Address strobe output: Valid when the address strobe output is permitted.
135	P47	I	General-purpose I/O port
	SYSCLK		System clock output: Valid when the system clock output specification is permitted. A clock with the same frequency as that external bus operation frequency is output at this pin (Clock output stops at transition to the STOP state).
122	P50	M	General-purpose I/O port : Valid when the data input specification is prohibited on LIN-UART2.
	SIN4		LIN-UART2 data input. Because this input is used as necessary while LIN-UART2 is used for input operation, the port output needs to be disabled except when it is used intentionally.
	CK0		External clock input for free-run timer 0
	CS0X		Chip select 0 output: Valid when the chip select 0 is permitted to output.

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Pin No.	Pin name	I/O circuit type*	Function
123	P51	I	General-purpose I/O port: Valid when the data output specification is prohibited on LIN-UART2.
	SOT4		LIN-UART2 data output: Valid when the data output specification is permitted on LIN-UART2.
	CS1X		Chip select 1 output: Valid when the output specification is permitted on chip select 1.
124	P52	I	General-purpose I/O port: Valid when clock output is prohibited on LIN-UART2.
	SCK4		LIN-UART2 clock input/output: Valid when the clock output specification is permitted on LIN-UART2.
	CS2X		Chip select 2 output: Valid when the output specification is permitted on chip select 2.
125	P53	M	General-purpose I/O port: Valid when the data input specification is prohibited on LIN-UART3.
	SIN5		LIN-UART3 data input. Because this input is used as necessary while LIN-UART3 is used for input operation, the port output needs to be disabled except when it is used intentionally.
	CK1		External clock input for free-run timer 1
	CS3X		Chip select 3 output: Valid when the output specification is permitted on chip select 3.
130	P54	I	General-purpose I/O port: Valid when data output specification is prohibited on LIN-UART3.
	SOT5		LIN-UART3 data output: Valid when the data output specification is permitted on LIN-UART3.
	RDX		External bus read strobe output: Valid at the external bus mode.
131	P55	I	General-purpose I/O port: Valid when clock output is prohibited on LIN-UART3.
	SCK5		LIN-UART3 clock input/output: Valid when the clock output specification is permitted on LIN-UART3.
	WR0X		External bus write strobe output: Valid when the WR0X output is permitted at the external bus mode.
132	P56	I	General-purpose I/O port
	OUT0		Output compare output
	WR1X		External bus write strobe output: Valid when the WR1X output is permitted at the external bus mode.
133	P57	J	General-purpose I/O port
	OUT1		Output compare output
	RDY		External ready input: Valid when the external ready input specification is permitted.

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Pin No.	Pin name	I/O circuit type*	Function
73 to 80	P60 to P67	E	General-purpose I/O ports: Valid when analog input specification is prohibited.
	AN0 to AN7		A/D converter analog inputs: Valid when the analog input is selected in the ADER register.
109	P70	I	General-purpose I/O port
	INT6		External interrupt input. Because this input is used as necessary while the pertinent external interrupt is enabled, the pot output need to be disabled except when it is used intentionally.
	RX0		RX0 input pin for CAN0
110	P71	I	General-purpose I/O port
	TX0		TX0 input pin for CAN0
111	P72	I	General-purpose I/O port
	INT7		External interrupt input. Because this input is used as necessary while the pertinent external interrupt is enabled, the pot output need to be disabled except when it is used intentionally.
	RX1		RX1 input pin for CAN1
112	P73	I	General-purpose I/O port
	TX1		TX1 output pin for CAN1
69 to 65	P80 to P84	E	General-purpose I/O port: Valid when analog input specification is prohibited.
	AN16 to AN20		A/D converter analog inputs: Valid when the analog input is selected in the ADER register.
64	P85	E	General-purpose I/O port: Valid when analog input specification is prohibited.
	AN21		A/D converter analog inputs: Valid when the analog input is selected in the ADER register.
	INT3		External interrupt input. Because this input is used as necessary while the pertinent external interrupt is enabled, the pot output need to be disabled except when it is used intentionally.
63	P86	E	General-purpose I/O port: Valid when analog input specification is prohibited.
	AN22		A/D converter analog inputs: Valid when the analog input is selected in the ADER register.
	INT4		External interrupt input. Because this input is used as necessary while the pertinent external interrupt is enabled, the pot output need to be disabled except when it is used intentionally.

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Pin No.	Pin name	I/O circuit type*	Function
62	P87	E	General-purpose I/O port: Valid when analog input specification is prohibited.
	AN23		A/D converter analog inputs: Valid when the analog input is selected in the ADER register.
	INT5		External interrupt input. Because this input is used as necessary while the pertinent external interrupt is enabled, the pot output need to be disabled except when it is used intentionally.
61	P90	L	General-purpose I/O port
	DA0		D/A converter analog output
60	P91	L	General-purpose I/O port
	DA1		D/A converter analog output
59	P92	I	General-purpose I/O port
	SGA0		Sound generator 0 output
58	P93	I	General-purpose I/O port
	SGO0		Sound generator 0 output
57	P94	I	General-purpose I/O port
	SGA1		Sound generator 1 output
56	P95	I	General-purpose I/O port
	SGO1		Sound generator 1 output
55	P96	I	General-purpose I/O port
	SGA2		Sound generator 2 output
54	P97	I	General-purpose I/O port
	SGO2		Sound generator 2 output
91	PA0	H	General-purpose I/O port
	PWM1P3		Stepping motor controller PWM output pin
92	PA1	H	General-purpose I/O port
	PWM1M3		Stepping motor controller PWM output pin
93	PA2	H	General-purpose I/O port
	PWM2P3		Stepping motor controller PWM output pin
94	PA3	H	General-purpose I/O port
	PWM2M3		Stepping motor controller PWM output pin
40	PB0	I	General-purpose I/O port
	PPG8H		PPG timer 8 output: Valid when the output specification is permitted on PPG timer 8.
41	PB1	I	General-purpose I/O port
	PPG9H		PPG timer 9 output: Valid when the output specification is permitted on PPG timer 9.

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Pin No.	Pin name	I/O circuit type*	Function
42	PB2	I	General-purpose I/O port
	PPG10H		PPG timer 10 output: Valid when the output specification is permitted on PPG timer 10.
43	PB3	I	General-purpose I/O port
	PPG11H		PPG timer 11 output: Valid when the output specification is permitted on PPG timer 11.
44	PB4	H	General-purpose I/O port
	PWM1P1		Stepping motor controller PWM output pin
45	PB5	H	General-purpose I/O port
	PWM1M1		Stepping motor controller PWM output pin
46	PB6	H	General-purpose I/O port
	PWM2P1		Stepping motor controller PWM output pin
47	PB7	H	General-purpose I/O port
	PWM2M1		Stepping motor controller PWM output pin
48	PC0	H	General-purpose I/O port
	PWM1P0		Stepping motor controller PWM output pin
49	PC1	H	General-purpose I/O port
	PWM1M0		Stepping motor controller PWM output pin
50	PC2	H	General-purpose I/O port
	PWM2P0		Stepping motor controller PWM output pin
51	PC3	H	General-purpose I/O port
	PWM2M0		Stepping motor controller PWM output pin
136	PD0	K	General-purpose I/O port
	TIN0		External event input pin for reload timer 0
	IN0		Trigger input for input capture 0: Valid when input capture trigger input is permitted and an input port is specified. If this pin is selected for input capture input, it is used as necessary for input. Therefore the port output needs to be disabled except when it is used intentionally.
	PWC0		PWC0 pulse width counter 0 input: Valid when the PWC0 pulse width counter 0 input is permitted.
	INT2		External interrupt input. Because those inputs are used as necessary while the pertinent external interrupt is enabled, the port outputs need to be disabled except when they are used intentionally.
	V0		LCD driver power supply input pin

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Pin No.	Pin name	I/O circuit type*	Function
137	PD1	K	General-purpose I/O port
	TIN1		External event input pin for reload timer 1
	IN1		Trigger input for input capture 1: Valid when input capture trigger input is permitted and an input port is specified. If this pin is selected for input capture input, it is used as necessary for input. Therefore the port output needs to be disabled except when it is used intentionally.
	V1		LCD driver power supply input pin
138	PD2	K	General-purpose I/O port
	TIN2		External event input pin for reload timer 2
	IN2		Trigger input for input capture 2: Valid when input capture trigger input is permitted and an input port is specified. If this pin is selected for input capture input, it is used as necessary for input. Therefore the port output needs to be disabled except when it is used intentionally.
	V2		LCD driver power supply input pin
139	PD3	K	General-purpose I/O port
	IN3		Trigger input for input capture 3: Valid when input capture trigger input is permitted and an input port is specified. If this pin is selected for input capture input, it is used as necessary for input. Therefore the port output needs to be disabled except when it is used intentionally.
	V3		LCD driver power supply input pin Power supply pin for the embedded ladder resistor.
140	PD4	F	General-purpose I/O port
	COM0		COM0 output from LCDC
	PPG1H		PPG timer 1 output: Valid when the output specification is permitted on PPG timer 1.
141	PD5	F	General-purpose I/O port
	COM1		COM1 output from LCDC
	PPG3H		PPG timer 3 output: Valid when the output specification is permitted on PPG timer 3.
142	PD6	F	General-purpose I/O port
	COM2		COM2 output from LCDC
	PPG5H		PPG timer 5 output: Valid when the output specification is permitted on PPG timer 5.
143	PD7	F	General-purpose I/O port
	COM3		COM3 output from LCDC
	PPG7H		PPG timer 7 output: Valid when the output specification is permitted on PPG timer 7.
95	PE0	H	General-purpose I/O port
	PWM1P2		Stepping motor controller PWM output pin

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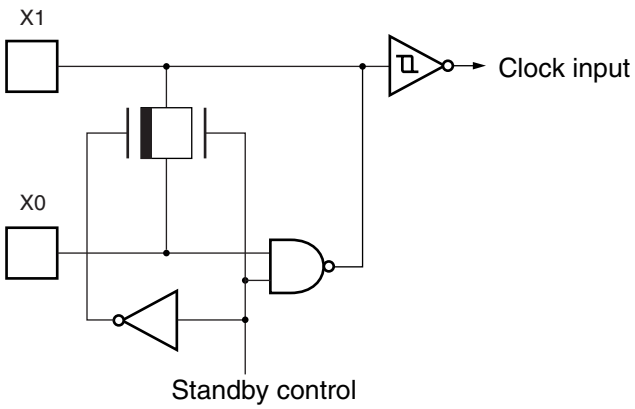
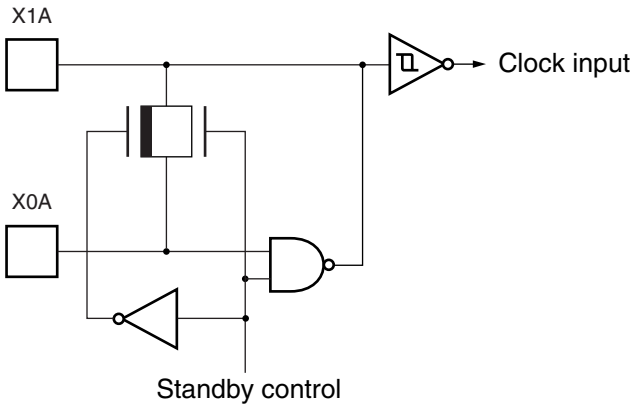
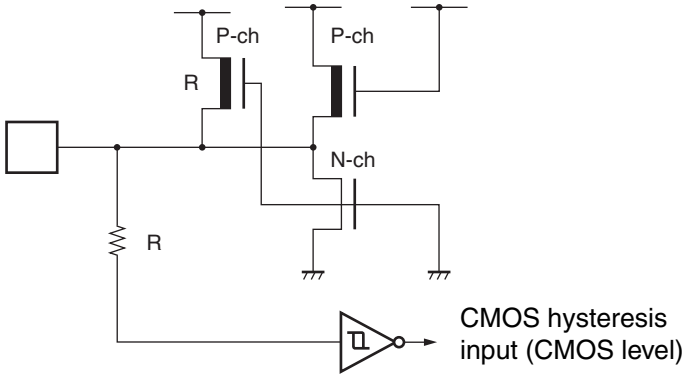
Pin No.	Pin name	I/O circuit type*	Function
96	PE1	H	General-purpose I/O port
	PWM1M2		Stepping motor controller PWM output pin
97	PE2	H	General-purpose I/O port
	PWM2P2		Stepping motor controller PWM output pin
98	PE3	H	General-purpose I/O port
	PWM2M2		Stepping motor controller PWM output pin
99	PE4	N	General-purpose I/O port
	PPG12H		PPG timer 12 output: Valid when the output specification is permitted on PPG timer 12.
	SDA0		I^2C0 serial data input/output pin
100	PE5	N	General-purpose I/O port
	PPG13H		PPG timer 13 output: Valid when the output specification is permitted on PPG timer 13.
	SCL0		I^2C0 serial clock input/output pin
101	PE6	N	General-purpose I/O port
	PPG14H		PPG timer 14 output: Valid when the output specification is permitted on PPG timer 14.
	SDA1		I^2C1 serial data input/output pin
102	PE7	N	General-purpose I/O port
	PPG15H		PPG timer 15 output: Valid when the output specification is permitted on PPG timer 15.
	SCL1		I^2C1 serial clock input/output pin
81 to 88	PF0 to PF7	E	General-purpose I/O ports: Valid when analog input is prohibited.
	AN8 to AN15		A/D converter analog inputs: Valid when the analog input is selected in the ADER register.
37	PG0	I	General-purpose I/O port.
	PPG0H		PPG timer 0 output: Valid when the output specification is permitted on PPG timer 0.
113	PG1	I	General-purpose I/O port
	TOT0		External timer output for reload timer 0
	PPG2H		PPG timer 2 output: Valid when the output specification is permitted on PPG timer 2.
114	PG2	I	General-purpose I/O port
	TOT1		External timer output for reload timer 1
	PPG4H		PPG timer 4 output: Valid when the output specification is permitted on PPG timer 4.
115	PG3	I	General-purpose I/O port
	TOT2		External timer output for reload timer 2
	PPG6H		PPG timer 6 output: Valid when the output specification is permitted on PPG timer 6.

* : For information about the I/O circuit type, refer to “■ I/O CIRCUIT TYPE”.

[Power supply and GND pins]

Pin No.	Pin name	Function
19, 127	VSS	GND pins. The potentials of these pins must be the same.
18, 126	VCC	Power supply pins. The potentials of these pins must be the same.
70	AVCC	Analog power supply pin for A/D converter
71	AVRH	Analog reference power supply pin for A/D converter
72	AVSS/AVRL	Analog GND or analog reference power supply pin for A/D converter
20	VCC3C	Capacitor coupling pin for internal regulator
38, 52, 89, 103	DVCC	Power supply pins for stepping motor controller
39, 53, 90, 104	DVSS	GND pins for stepping motor controller

■ I/O CIRCUIT TYPE

Group	Circuit Type	Remarks
A		For high speed (source oscillation of main clock) • Oscillation circuit • Feedback resistance X0 : approx. 1 MΩ
B		For low speed (source oscillation of sub clock) • Oscillation circuit • Feedback resistance X0A : approx. 7 MΩ
C		• Hysteresis (CMOS level) input • Pull-up resistor supported Pull-up resistor value = approx. 50 kΩ • No standby control

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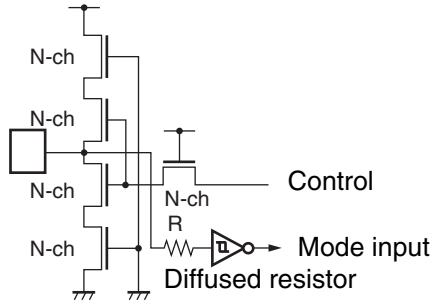
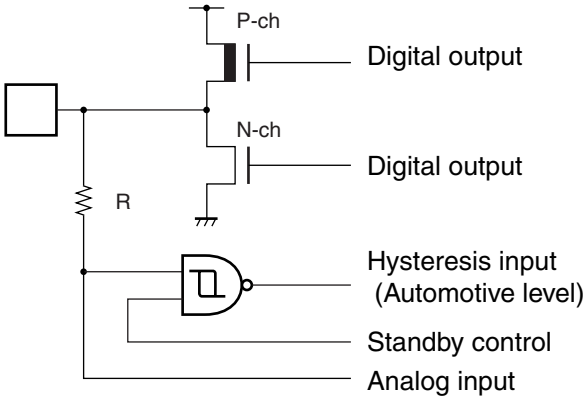
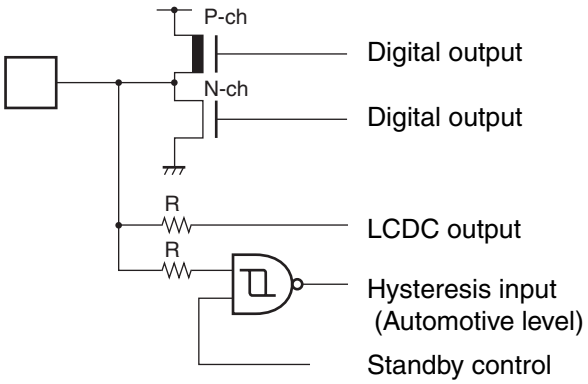
Group	Circuit Type	Remarks
D		• Flash memory product Hysteresis input High-voltage control for Flash test supported
E		• CMOS output (4 mA) • Hysteresis (Automotive level) input (Standby control supported) • Analog input (Analog input is valid when the corresponding ADER bit is set to 1.)
F		• CMOS output (4 mA) • LCDC output • Hysteresis (Automotive level) input (Standby control provided)

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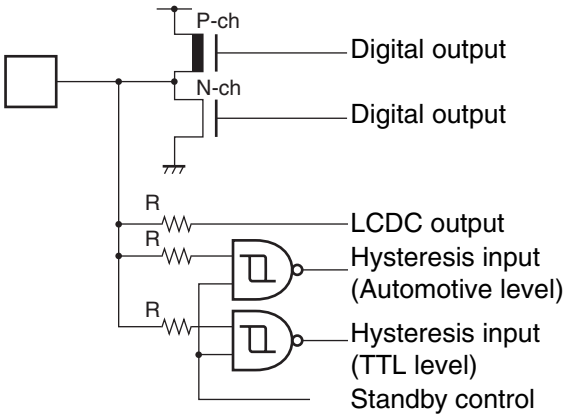
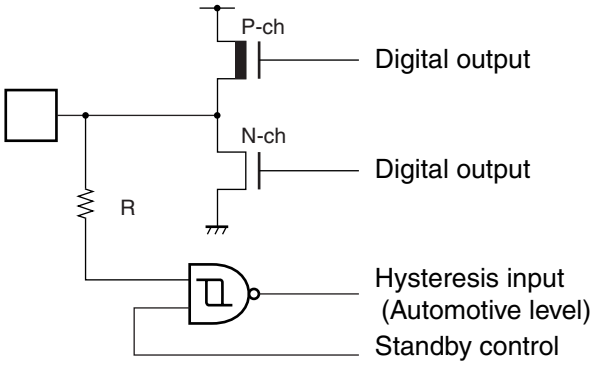
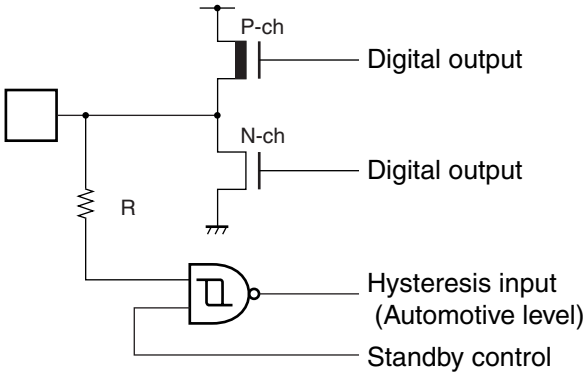
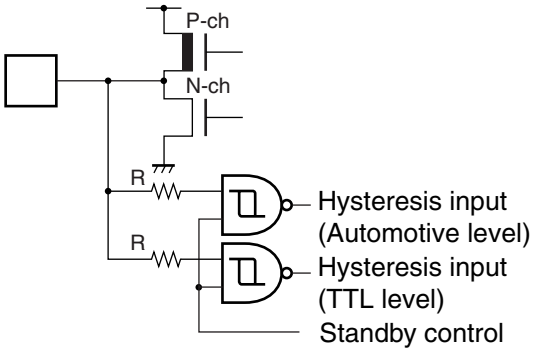
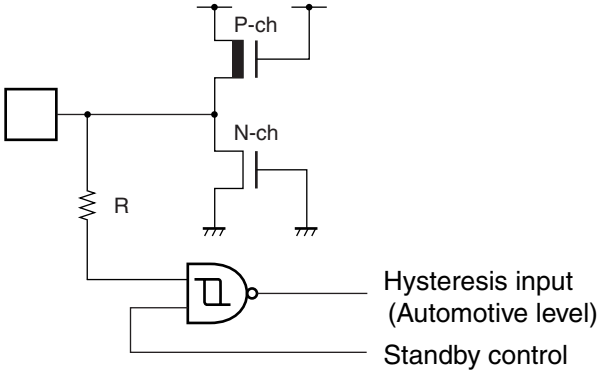
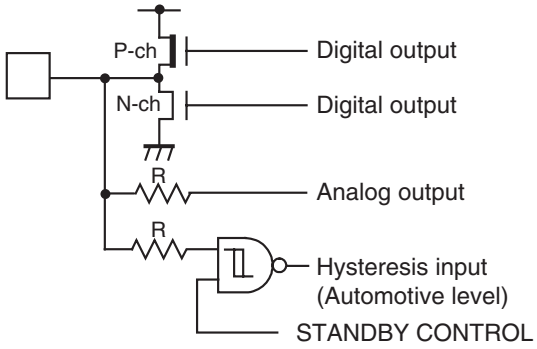
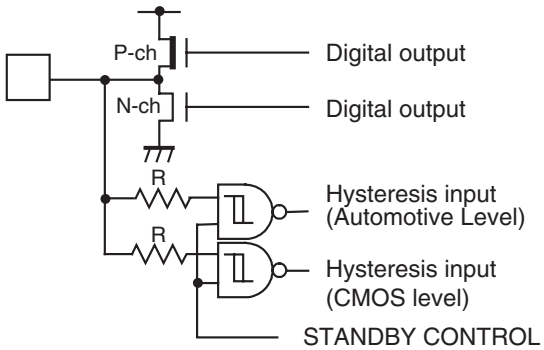
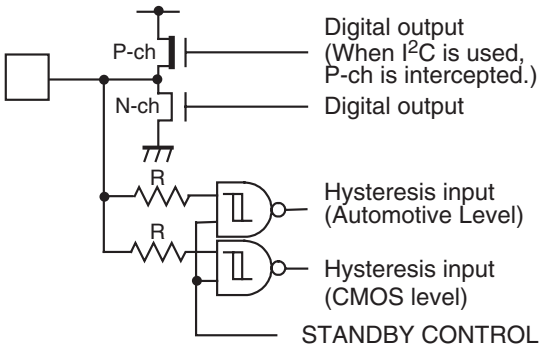
Group	Circuit Type	Remarks
G		• CMOS output (4 mA) • LCDC output • Hysteresis (Automotive level) input (Standby control supported) • Hysteresis (TTL level) input (Standby control supported)
H		• CMOS output High current output for PWM (30 mA) • Hysteresis (Automotive level) input (Standby control supported)
I		• CMOS output (4 mA) • Hysteresis (Automotive level) input (Standby control supported)

(Continued)

Group	Circuit Type	Remarks
J		• CMOS output (4 mA) • Hysteresis (Automotive level) input (Standby control supported) • Hysteresis (TTL level) input (Standby control supported)
K		Hysteresis (Automotive level) input (Standby control supported)

(Continued)

(Continued)

Group	Circuit Type	Remarks
L		• CMOS output (4 mA) • D/A converter output • Hysteresis (automotive level) input (Standby control supported)
M		• CMOS output (4 mA) • Hysteresis (automotive level) input (standby control supported) • Hysteresis (CMOS level) input (Standby control supported)
N		• CMOS output (3 mA) • Hysteresis (automotive level) input (Standby control supported) • Hysteresis (CMOS level) input (Standby control supported)

■ HANDLING DEVICES

• Preventing Latch-up

Latch-up may occur in a CMOS IC, if a voltage greater than V_{CC} or less than V_{SS} is applied to input and output pin, or if an above-rating voltage is applied between VCC and VSS pins. When latch-up occurs, it may significantly increase the power supply current, and may cause thermal destruction of an element. When you use a CMOS IC, be very careful not to exceed the maximum rating.

• Treatment of Unused Input Pins

Do not leave unused input pins open, as this may cause a malfunction. Handle by performing a pull-up or pull-down with a resistance of 2 kΩ or more. An unused I/O pin should be set to the output status and left open. When set to the input status, it should be handled in the same way as an input pin.

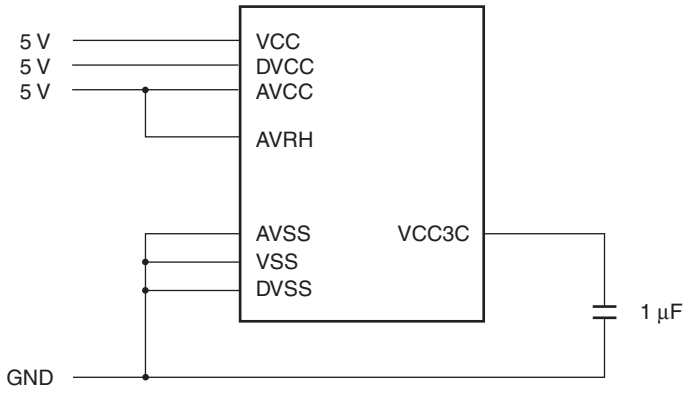
• Power supply pins

If there are multiple VCC and VSS pins, from the point of view of device design pins to be of the same potential are connected inside the device to prevent such malfunctioning as latch-up. However, you must connect all the pins to the external power supply and ground lines to lower the electro-magnetic emission level, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total output current rating. Moreover, connect the current supply source to the VCC and VSS pins of this device via a low impedance.

Furthermore, it is also advisable to connect a ceramic bypass capacitor of approximately 0.1 μF between VCC and VSS near this device.

This device incorporates a regulator. When using the device with 5 V power supply, apply that power supply to the VCC pin and always connect the VCC3C pin to a capacitor with 1 μF or more for the purpose of regulator.

• Example of power supply connection



- Crystal oscillator circuit

  Noise near the X0/X1 pins and X0A/X1A pins may cause the device to malfunction. Design the PC board such that X0/X1 pins, X0A/X1A pins, the crystal oscillator (or ceramic oscillator), and the bypass capacitor to the ground are placed as near one another as possible. When routing the X0 and X1 signals, they should be shielded for use on the board. Caution must be taken especially when using a pin next to the X0.

  It is strongly recommended that the PC board artwork be designed such that the X0, X1, X0A and X1A pins are surrounded by ground plane because stable operation can be expected with such a layout.

  In addition, the X0A/X1A pins must be surrounded by ground plane even if the sub clock is disabled.

  When using MB91F223S, connect the X0A pin to GND and leave the X1A pin open.

  Please ask the crystal maker to evaluate the oscillational characteristics of the crystal and this device.

- Mode pins (MD0 to MD2)

  These pins should be connected directly to VCC or VSS pins. To prevent the device erroneously switching to test mode due to noise, design the PC board such that the distance between the mode pins and VCC or VSS pin is as short as possible and the connection impedance is now.

- Operation at start-up

  Always use the INITX pin to perform a setting initialization reset (INIT) after power-on. Immediately after power-on, hold the low level input to the INITX pin for the stabilization wait time required for the oscillator circuit, to take the oscillation stabilization wait time for the oscillator circuit.

  For INIT via the INITX pin, the oscillation stabilization wait time setting is initialized to the minimum value.

- Source oscillation input upon power-on

  When power-on, always input the clock for the duration of the oscillation stabilization delay time.

- Treatment of power supply pins on A/D converter

  Connect to ensure “AV_{CC} = AVRH = V_{CC} and AV_{SS} = V_{SS}” even if the A/D converter is not in use.

- Power-on sequence for power supply analog input of A/D converter

  Always supply power to the A/D converter (AVCC and AVRH) and apply analog input (AN0 to AN 23) after turning on the digital power supply (VCC). Also, turn off the power supply for the A/D converter and analog input before turning off the digital power supply (VCC). AVR should not exceed AV_{CC} when turning on and off. Even when using a pin shared with analog input as an input port, ensure that the input voltage does not exceed AV_{CC}.

- Handling power supply for high-current output buffer pin (DVCC, DVSS)

  Always apply power to high-current output buffer pins (DVCC) after turning on the digital power supply (VCC). In addition, turn off the power supply for the high-current output buffer pins before turning off the digital power supply (VCC).

  Apply the same power as for high-current output buffer pins even when using such pins as general-purpose ports (There is no problem in turning on or off the power supply for the high-current output buffer pins and the digital power supply at the same time).

  Always use the GND pin (DVSS) for the high-current output buffer pin at the same potential as the digital GND pin (VSS).

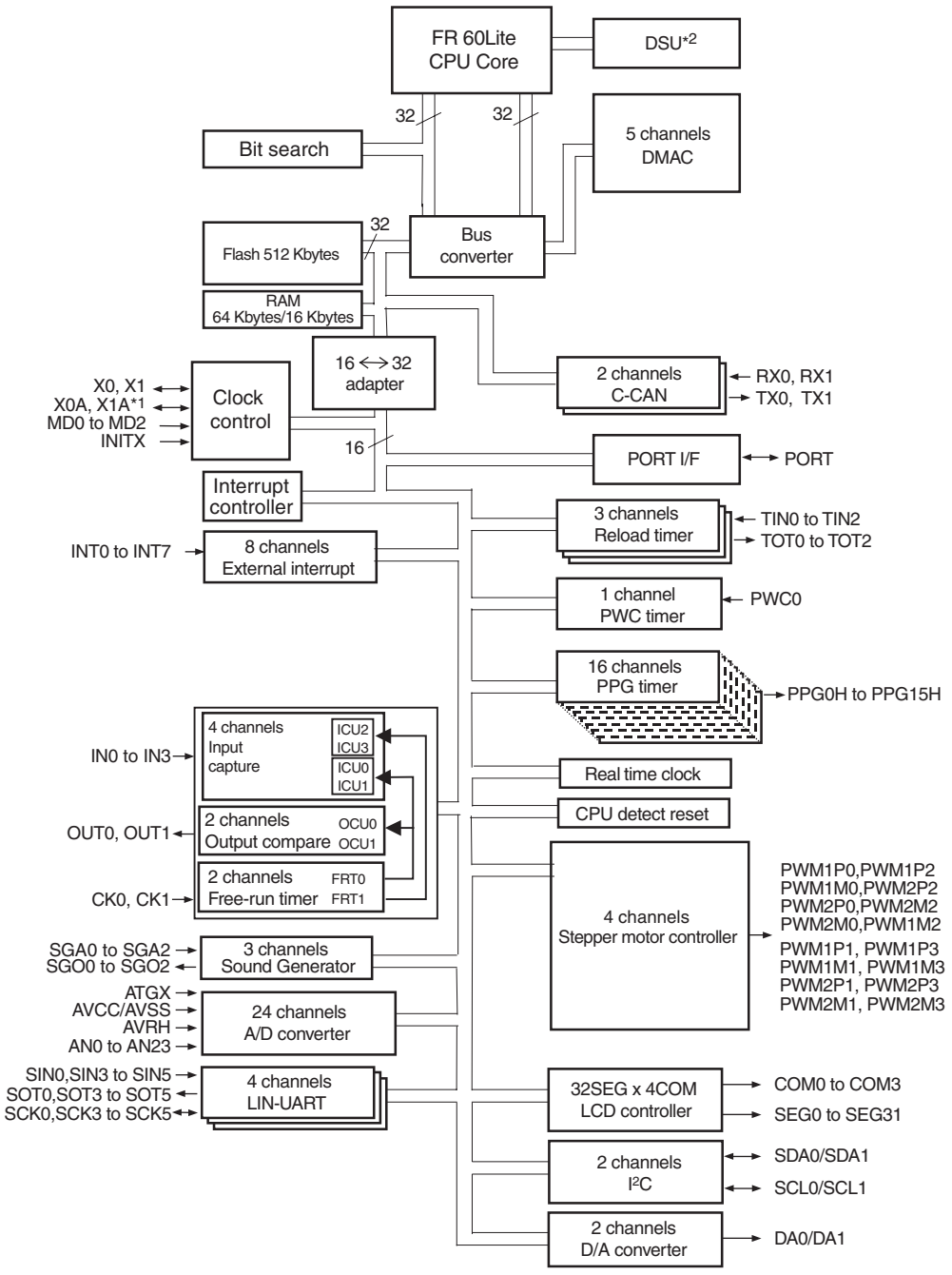
- Switching from main clock mode to sub clock mode or stop mode

  Always stop the main clock after switching the main clock mode to the sub clock mode or stop mode. Also secure the oscillation stabilization wait time when returning from the sub clock mode or stop mode to the main clock mode.

- Flash write

  Note that Flash write is not possible in the sub mode.

■ BLOCK DIAGRAM



*1 : The devices with an S suffix in the part number does not support the sub-block.

*2 : DSU is built into the MB91V220 only.

■ MEMORY SPACE

• Memory space

The FR family has 4 Gbytes logical address space (2^{32} addresses) linearly accessible to the CPU space.

• Direct addressing area

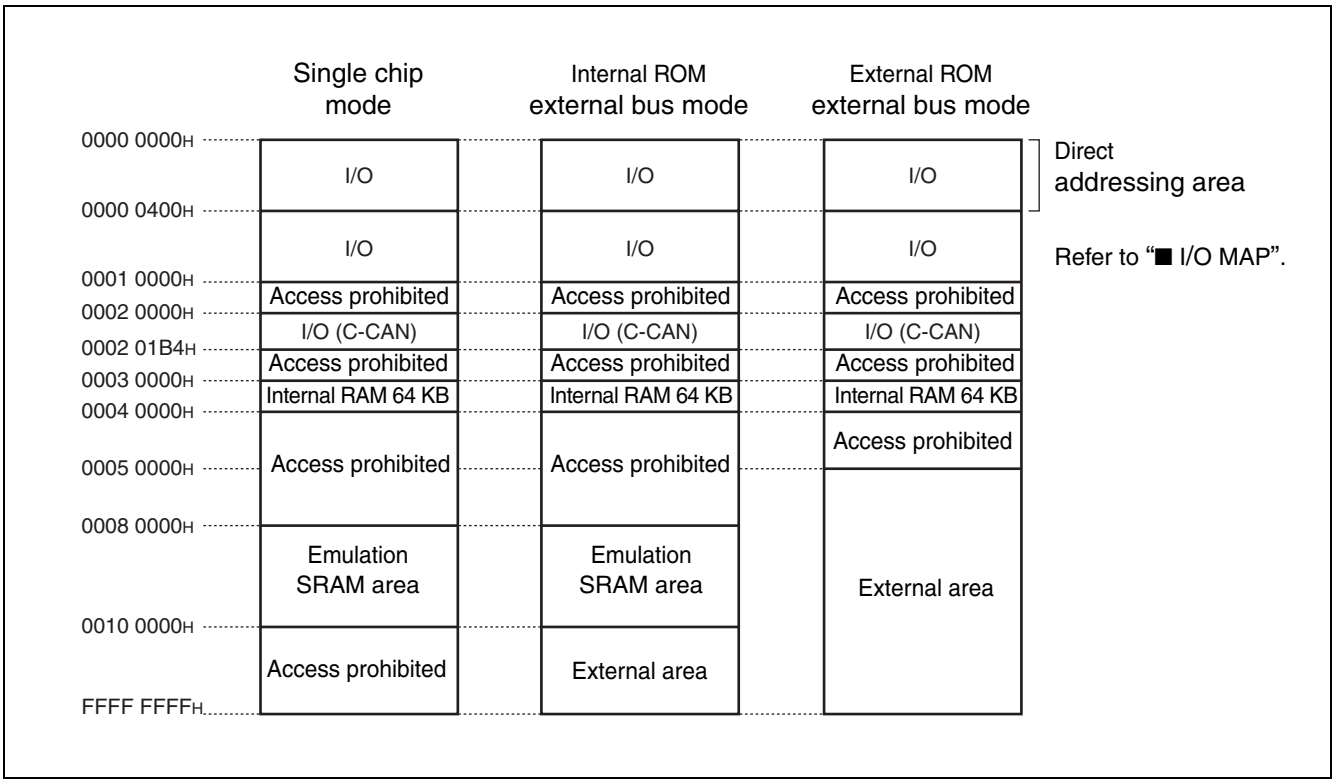
The following address space areas are used as I/O areas.

These areas are called direct addressing areas, in which the address of an operand can be specified directly during on instruction.

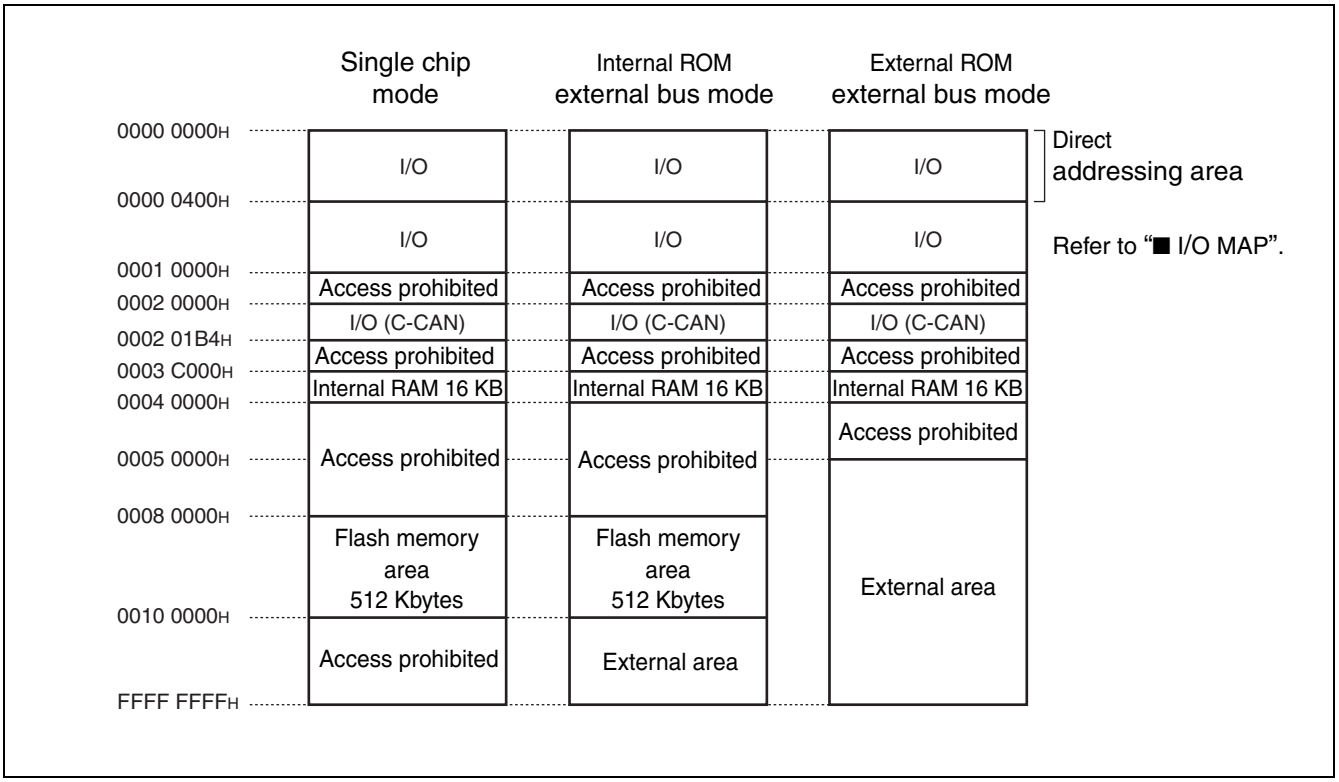
The direct area varies depending on the size of data to be accessed as follows.
→ Byte data access : 000_H to $0FF_H$
→ Halfword data access : 000_H to $1FF_H$
→ Word data access : 000_H to $3FF_H$

■ MEMORY MAP

MB91V220



MB91F223/S



Note : Each mode is set depending on the mode vector fetch after INITX is negated. For mode settings, refer to "■ MODE SETTINGS".

■ MODE SETTINGS

The FR family, sets the operation mode using mode pins (MD2 to MD0) and mode data.

• Mode pins

The mode pins (MD2 to MD0) specify how the mode vector fetch and reset vector fetch is performed.

Other settings than these in the table are prohibited.

Mode pin			Mode name	Reset vector access area
MD2	MD1	MD0		
0	0	0	Internal ROM mode vector	Internal

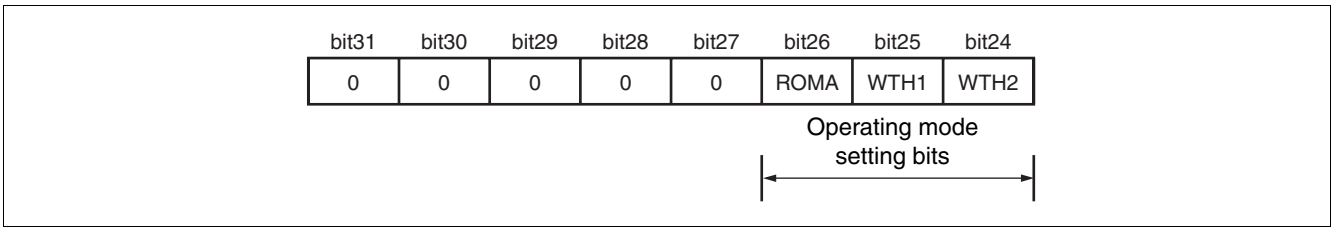
• Mode data

Data written to the internal mode register (MODR) by mode vector fetch is called mode data.

After an operating mode has been set in the mode register the device operates in that operating mode.

The mode data is set by all reset sources. User programs cannot set data to the mode register.

Details of mode data



Bit 31 to bit 27 are reserved.

Always set the value to "00000B". Otherwise, the operation is not guaranteed.

[bit26] ROMA (Internal ROM enabling bit)

This bit specifies whether to enable internal ROM area.

ROMA	Function	Remarks
0	External ROM mode	Internal F-bus RAM is enabled, and the internal ROM area (80000H to 100000H) becomes an external area.
1	Internal ROM mode	Internal ROM area is enabled.

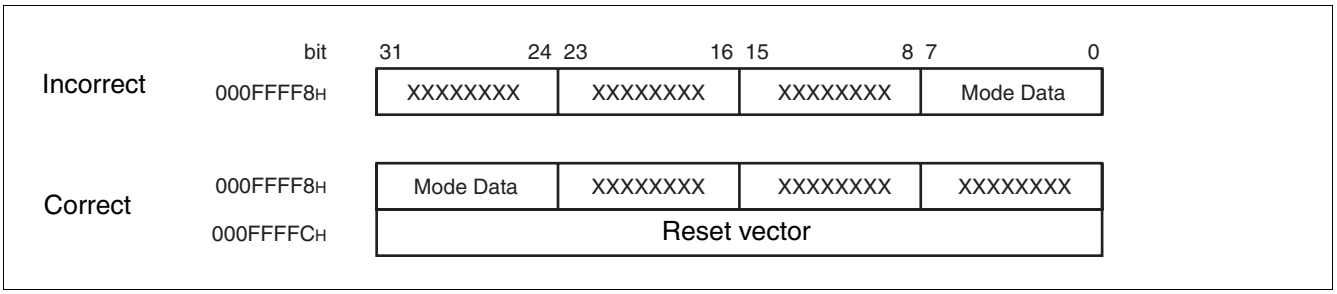
[bit25, bit24] WTH1, WTH0 (bus width setting bits)

Specify the bus width for the external bus mode.

In the external bus mode, this value is set to DBW1 and DBW0 bits in ACR0 (CS0 area).

WTH1	WTH0	Function
0	0	8-bit bus width
0	1	16-bit bus width
1	0	—
1	1	Single chip mode

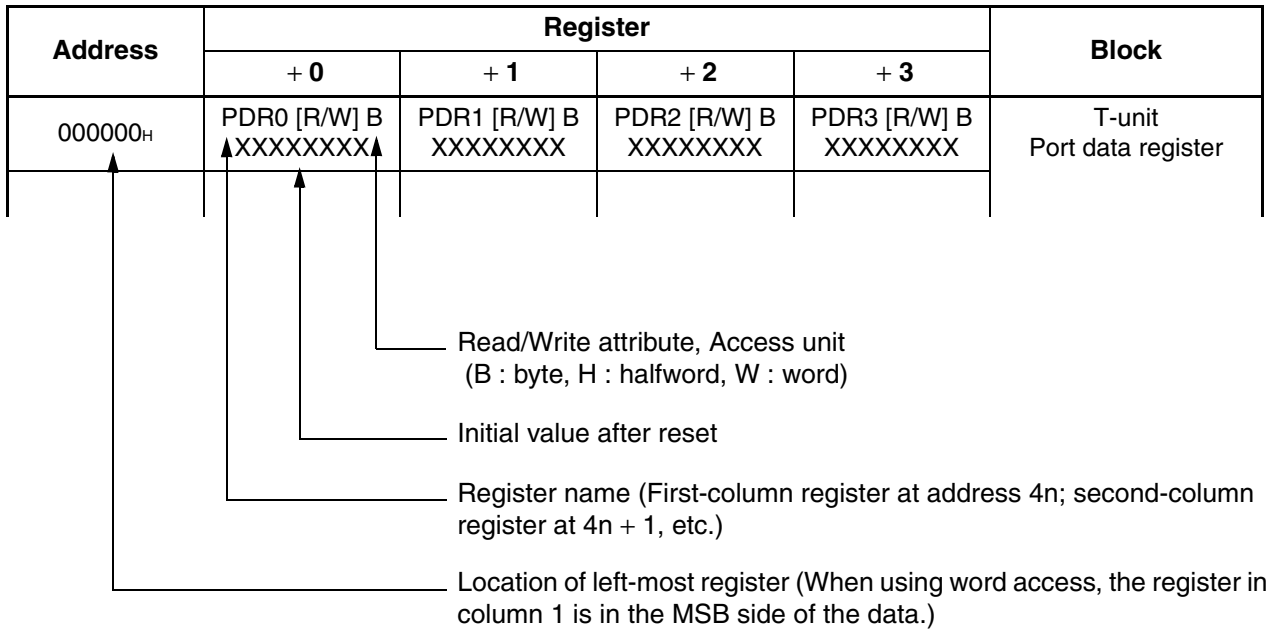
Note : Mode data set in the mode vector must be placed as byte data at 000FFFF8H.
Place the data in the most significant byte from bit 31 to bit 24 as the FR family uses the big endian system for byte endian.



■ I/O MAP

The following table shows the correspondence between the memory space area and each register of the peripheral resource.

[How to read the map]



Note :

Initial values of register bits are represented as follows :

“ 1 ” : Initial value “1”

“ 0 ” : Initial value “0”

“ X ” : Initial value “undefined”

“ - ” : No physical register present at this location

Access by any undescribed data access attribute is prohibited.

Address	Register				Block
	+0	+1	+2	+3	
00000000H	PDR0[R/W] B,H XXXXXXXX	PDR1[R/W] B,H XXXXXXXX	PDR2[R/W] B,H XXXXXXXX	PDR3[R/W] B,H XXXXXXXX	Port Data Register
00000004H	PDR4[R/W] B,H XXXXXXXX	PDR5[R/W] B,H XXXXXXXX	PDR6[R/W] B,H XXXXXXXX	PDR7[R/W] B,H ----XXXX	
00000008H	PDR8[R/W] B,H XXXXXXXX	PDR9[R/W] B,H XXXXXXXX	PDRA[R/W] B,H ----XXXX	PDRB[R/W] B,H XXXXXXXX	
0000000CH	PDRC[R/W] B,H ----XXXX	PDRD[R/W] B,H 0000XXXX	PDRE[R/W] B,H XXXXXXXX	PDRF[R/W] B,H XXXXXXXX	
00000010H	PDRG[R/W] B,H ----XXXX	-	-	-	
00000014H to 0000003CH	-				Reserved
00000040H	EIRR0 [R/W] B,H,W XXXXXXXX	ENIR0 [R/W] B,H,W 00000000	ELVR0 [R/W] B,H,W 00000000 00000000		External Interrupt
00000044H	DICR [R/W] B,H,W -------0	HRCL[R/W] B 0--11111	-		Delayed Interrupt
00000048H	TMRLR0[W] H,W XXXXXXXX XXXXXXXX		TMR0[R] H,W XXXXXXXX XXXXXXXX		Reload Timer 0
0000004CH	-	Reserved	TMCSR0[R/W] B,H,W ----0000 00000000		
00000050H	TMRLR1[W] H,W XXXXXXXX XXXXXXXX		TMR1[R] H,W XXXXXXXX XXXXXXXX		Reload Timer 1
00000054H	-		TMCSR1[R/W] B,H,W ----0000 00000000		
00000058H	TMRLR2[W] H,W XXXXXXXX XXXXXXXX		TMR2[R] H,W XXXXXXXX XXXXXXXX		Reload Timer 2
0000005CH	-		TMCSR2[R/W] B,H,W ----0000 00000000		
00000060H to 00000064H	-				Reserved
00000068H	DACR1[R/W] B, H, W -------0	DACR0[R/W] B, H, W -------0	DADR1[R/W] B, H, W XXXXXXXX	DADR0[R/W] B, H, W XXXXXXXX	DAC
0000006CH to 0000007CH	-				Reserved

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
00000080H	-	SGDBL0[R/W] B,H,W -------0	SGCR0[R/W] B,H,W 0-----00 000--000		Sound Generator 0
00000084H	SGAR0[R/W] B,H,W 00000000	SGFR0[R/W] B,H,W XXXXXXXX	SGTR0[R/W] B,H,W XXXXXXXX	SGDR0[R/W] B,H,W XXXXXXXX	
00000088H	-	SGDBL1[R/W] B,H,W -------0	SGCR1[R/W] B,H,W 0-----00 000--000		Sound Generator 1
0000008CH	SGAR1[R/W] B,H,W 00000000	SGFR1[R/W] B,H,W XXXXXXXX	SGTR1[R/W] B,H,W XXXXXXXX	SGDR1[R/W] B,H,W XXXXXXXX	
00000090H	-	SGDBL2[R/W] B,H,W -------0	SGCR2[R/W, R] B,H,W 0------00 000--000		Sound Generator 2
00000094H	SGAR2[R/W] B,H,W 00000000	SGFR2[R/W] B,H,W XXXXXXXX	SGTR2[R/W] B,H,W XXXXXXXX	SGDR2[R/W] B,H,W XXXXXXXX	
00000098H	LCDCMR[R/W] B,H,W ----0000	-	LCR0 [R/W] B,H,W 00010000	LCR1 [R/W] B,H,W 00000000	LCD Controller Driver
0000009CH	VRAM0 [R/W] B,H,W XXXXXXXX	VRAM1[R/W] B,H,W XXXXXXXX	VRAM2 [R/W] B,H,W XXXXXXXX	VRAM3 [R/W] B,H,W XXXXXXXX	
000000A0H	VRAM4 [R/W] B,H,W XXXXXXXX	VRAM5 [R/W] B,H,W XXXXXXXX	VRAM6 [R/W] B,H,W XXXXXXXX	VRAM7 [R/W] B,H,W XXXXXXXX	
000000A4H	VRAM8 [R/W] B,H,W XXXXXXXX	VRAM9 [R/W] B,H,W XXXXXXXX	VRAM10[R/W] B,H,W XXXXXXXX	VRAM11[R/W] B,H,W XXXXXXXX	
000000A8H	VRAM12[R/W] B,H,W XXXXXXXX	VRAM13[R/W] B,H,W XXXXXXXX	VRAM14[R/W] B,H,W XXXXXXXX	VRAM15[R/W] B,H,W XXXXXXXX	
000000ACH	-				Reserved
000000B0H	SCR3 [R/W] B,H,W 00000000	SMR3 [R/W] B,H,W 00000000	SSR3 [R/W] B,H,W 00001000	RDR3 [R/W] B,H,W 00000000	LIN-UART1
000000B4H	ESCR3[R/W] B,H,W 00000X00	ECCR3[R/ W] B,H,W 000000XX	BGR13[R/W] B,H,W XXXXXXXX	BGR03[R/W] B,H,W XXXXXXXX	
000000B8H	SCR4 [R/W] B,H,W 00000000	SMR4 [R/W] B,H,W 00000000	SSR4 [R/W] B,H,W 00001000	RDR4 [R/W] B,H,W 00000000	LIN-UART2
000000BCH	ESCR4[R/W] B,H,W 00000X00	ECCR4[R/W] B,H,W 000000XX	BGR14[R/W] B,H,W XXXXXXXX	BGR04[R/W] B,H,W XXXXXXXX	

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
000000C0H	SCR5 [R/W] B,H,W 00000000	SMR5 [R/W] B,H,W 00000000	SSR5 [R/W] B,H,W 00001000	RDR5 [R/W] B,H,W 00000000	LIN-UART3
000000C4H	ESCR5[R/W] B,H,W 00000X00	ECCR5[R/W] B,H,W 000000XX	BGR15[R/W] B,H,W XXXXXXXX	BGR05 [R/W] B,H,W XXXXXXXX	
000000C8H	SCR0 [R/W] B,H,W 00000000	SMR0 [R/W] B,H,W 00000000	SSR0 [R/W, R] B,H,W 00001000	RDR0 [R/W] B,H,W 00000000	LIN-UART0
000000CCH	ESCR0[R/W] B,H,W 00000X00	ECCR0[R/W] B,H,W 000000XX	BGR10[R/W] B,H,W XXXXXXXX	BGR00[R/W] B,H,W XXXXXXXX	
000000D0H	-				Reserved
000000D4H	TCDT0 [R/W] H,W 00000000 00000000		-	TCCS0 [R/W] B,H,W 00000000	16-bit Free-Run Timer 0
000000D8H	TCDT1 [R/W] H,W 00000000 00000000		-	TCCS1 [R/W] B,H,W 00000000	16-bit Free-Run Timer 1
000000DCH to 000000E0H	-				Reserved
000000E4H	IPCP1 [R] H,W XXXXXXXX XXXXXXXX		IPCP0 [R] H,W XXXXXXXX XXXXXXXX		16-bit ICU 0, 1
000000E8H	-	-	-	ICS01 [R/W] B,H,W 00000000	
000000ECH	IPCP3 [R] H,W XXXXXXXX XXXXXXXX		IPCP2 [R] H,W XXXXXXXX XXXXXXXX		16-bit ICU 2, 3
000000F0H	-	-	-	ICS23 [R/W] B,H,W 00000000	
000000F4H to 00000104H	-				Reserved
00000108H	OCCP1 [R/W] H,W XXXXXXXX XXXXXXXX		OCCP0 [R/W] H,W XXXXXXXX XXXXXXXX		16-bit OCU 0, 1
0000010CH	-	-	-	-	
00000110H	-		OCS01 [R/W] B,H,W 11101100 00001100		
00000114H to 0000012CH	-				Reserved

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
00000130H	PWCSR0[R/W] B,H,W 0000000X 00000000		PWCR0[R] H,W 00000000 00000000		PWC
00000134H	-		-		
00000138H	-	PDIVR0[R/W] B,H,W -----000	-	-	
0000013CH to 00000140H	-				Reserved
00000144H	-	WTDBL [R/W] B -------0	WTCR [R/W] B,H 00000000 000-00-0		Real Time Clock
00000148H	-	WTBR [R/W] B ---XXXXX XXXXXXXX XXXXXXXX			
0000014CH	WTHR [R/W] B,H ---XXXXX	WTMR [R/W] B,H --XXXXXX	WTSR [R/W] B --XXXXXX	-	
00000150H	ADERH[R/W] B,H,W 11111111 11111111		ADERL[R/W] B,H,W 11111111 11111111		ADC
00000154H	ADCS1[R/W] B,H,W 00000000	ADCS0[R/W] B,H,W 00000000	ADCR1[R] B,H,W ------XX	ADCR0[R] B,H,W XXXXXXXX	
00000158H	ADCT1[R/W] B,H,W 00010000	ADCT0[R/W] B,H,W 00101100	ADSCH[R/W] B,H,W ---00000	ADECH[R/W] B,H,W ---00000	
0000015CH	CUCR[R/W] B,H,W -------- ---0--00		CUTD[R/W] B,H,W 10000000 00000000		Clock Calibrator
00000160H	CUTR1[R] B,H,W -------- 00000000		CUTR2[R] B,H,W 00000000 00000000		
00000164H	PWC20[R/W] H,W ------XX XXXXXXXX		PWC10[R/W] H,W ------XX XXXXXXXX		SMC0
00000168H	-	PWC0[R/W] B -0000--0	PWS20[R/W] B,H,W -0000000	PWS10[R/W] B,H,W --000000	
0000016CH	PWC21[R/W] H,W ------XX XXXXXXXX		PWC11[R/W] H,W ------XX XXXXXXXX		SMC1
00000170H	-	PWC1[R/W] B -0000--0	PWS21[R/W] B,H,W -0000000	PWS11[R/W] B,H,W --000000	
00000174H	PWC22[R/W] H,W ------XX XXXXXXXX		PWC12[R/W] H,W ------XX XXXXXXXX		SMC2
00000178H	-	PWC2[R/W] B -0000--0	PWS22[R/W] B,H,W -0000000	PWS12[R/W] B,H,W --000000	

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
0000017C$_H$	PWC23[R/W] H,W ------XX XXXXXXXX		PWC13[R/W] H,W ------XX XXXXXXXX		SMC3
00000180$_H$	-	PWC3[R/W] B -0000--0	PWS23[R/W] B,H,W -0000000	PWS13[R/W] B,H,W --000000	
00000184$_H$ to 000001A4$_H$	-				Reserved
000001A8$_H$	CANPRE[R/W] B,H,W 00000000	Reserved	-	-	CAN Prescaler
000001AC$_H$	-				Reserved
000001B0$_H$	-	TRG0[R/W] B,H,W 00000000	-	REVC0[R/W] B,H,W 00000000	PPG0
000001B4$_H$	PRLH0[R/W]B,H,W XXXXXXXX	PRLL0[R/W]B,H,W XXXXXXXX	PRLH1[R/W]B,H,W XXXXXXXX	PRLL1[R/W]B,H,W XXXXXXXX	
000001B8$_H$	PRLH2[R/W]B,H,W XXXXXXXX	PRLL2[R/W]B,H,W XXXXXXXX	PRLH3[R/W]B,H,W XXXXXXXX	PRLL3[R/W]B,H,W XXXXXXXX	
000001BC$_H$	PPGC0[R/W] B,H,W 0000000X	PPGC1[R/W] B,H,W 0000000X	PPGC2[R/W] B,H,W 0000000X	PPGC3[R/W] B,H,W 0000000X	
000001C0$_H$	PRLH4[R/W]B,H,W XXXXXXXX	PRLL4[R/W]B,H,W XXXXXXXX	PRLH5[R/W]B,H,W XXXXXXXX	PRLL5[R/W]B,H,W XXXXXXXX	
000001C4$_H$	PRLH6[R/W]B,H,W XXXXXXXX	PRLL6[R/W]B,H,W XXXXXXXX	PRLH7[R/W]B,H,W XXXXXXXX	PRLL7[R/W]B,H,W XXXXXXXX	
000001C8$_H$	PPGC4[R/W] B,H,W 0000000X	PPGC5[R/W] B,H,W 0000000X	PPGC6[R/W] B,H,W 0000000X	PPGC7[R/W] B,H,W 0000000X	
000001CC$_H$	-	-	-	-	
000001D0$_H$	TRG1[R/W] B,H,W 00000000	-	REVC1[R/W] B,H,W 00000000	-	PPG1
000001D4$_H$	PRLH8[R/W]B,H,W XXXXXXXX	PRLL8[R/W]B,H,W XXXXXXXX	PRLH9[R/W]B,H,W XXXXXXXX	PRLL9[R/W]B,H,W XXXXXXXX	
000001D8$_H$	PRLHA[R/W]B,H,W XXXXXXXX	PRLLA[R/W]B,H,W XXXXXXXX	PRLHB[R/W]B,H,W XXXXXXXX	PRLLB[R/W]B,H,W XXXXXXXX	
000001DC$_H$	PPGC8[R/W] B,H,W 0000000X	PPGC9[R/W] B,H,W 0000000X	PPGCA[R/W] B,H,W 0000000X	PPGCB[R/W] B,H,W 0000000X	
000001E0$_H$	PRLHC[R/W] B,H,W XXXXXXXX	PRLLC[R/W]B,H,W XXXXXXXX	PRLHD[R/W] B,H,W XXXXXXXX	PRLLD[R/W]B,H,W XXXXXXXX	

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
000001E4H	PRLHE[R/W]B,H,W XXXXXXXX	PRLLE[R/W]B,H,W XXXXXXXX	PRLHF[R/W]B,H,W XXXXXXXX	PRLLF[R/W]B,H,W XXXXXXXX	PPG1
000001E8H	PPGCC[R/W] B,H,W 0000000X	PPGCD[R/W] B,H,W 0000000X	PPGE[R/W]B,H,W 0000000X	PPGCF[R/W] B,H,W 0000000X	
000001ECH	-	-	-	-	
000001F0H to 000001FCH	-				Reserved
00000200H	DMACA0[R/W] B,H,W * 00000000 0000XXXX XXXXXXXX XXXXXXXX				DMAC
00000204H	DMACB0[R/W] B,H,W 00000000 00000000 XXXXXXXX XXXXXXXX				
00000208H	DMACA1[R/W] B,H,W * 00000000 0000XXXX XXXXXXXX XXXXXXXX				
0000020CH	DMACB1[R/W] B,H,W 00000000 00000000 XXXXXXXX XXXXXXXX				
00000210H	DMACA2[R/W] B,H,W * 00000000 0000XXXX XXXXXXXX XXXXXXXX				
00000214H	DMACB2[R/W] B,H,W 00000000 00000000 XXXXXXXX XXXXXXXX				
00000218H	DMACA3[R/W] B,H,W * 00000000 0000XXXX XXXXXXXX XXXXXXXX				
0000021CH	DMACB3[R/W] B,H,W 00000000 00000000 XXXXXXXX XXXXXXXX				
00000220H	DMACA4[R/W] B,H,W * 00000000 0000XXXX XXXXXXXX XXXXXXXX				
00000224H	DMACB4[R/W] B,H,W 00000000 00000000 XXXXXXXX XXXXXXXX				
00000228H to 0000023CH	Reserved				
00000240H	DMACR[R/W] B 0XX00000 XXXXXXXX XXXXXXXX XXXXXXXX				
00000244H to 000003ECH	-				Reserved

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
000003F0H	BSD0 [W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Bit Search
000003F4H	BSD1 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000003F8H	BSDC [W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000003FCH	BSRR [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00000400H	DDR0[R/W] B,H,W 00000000	DDR1[R/W] B,H,W 00000000	DDR2[R/W] B,H,W 00000000	DDR3[R/W] B,H,W 00000000	Data Direction Register
00000404H	DDR4[R/W] B,H,W 00000000	DDR5[R/W] B,H,W 00000000	DDR6[R/W] B,H,W 00000000	DDR7[R/W] B,H,W ----0000	
00000408H	DDR8[R/W] B,H,W 00000000	DDR9[R/W] B,H,W 00000000	DDRA[R/W] B,H,W ----0000	DDRB[R/W] B,H,W 00000000	
0000040CH	DDRC[R/W] B,H,W ----0000	DDRD[R/W] B,H,W 1111----	DDRE[R/W] B,H,W 00000000	DDRF[R/W] B,H,W 00000000	
00000410H	DDRG[R/W] B,H,W ----0000	-	-	-	
00000414H to 0000041CH	-				Reserved
00000420H	PFR0[R/W] B,H,W 00000000	PFR1[R/W] B,H,W 00000000	PFR2[R/W] B,H,W 00000000	PFR3[R/W] B,H,W 00000000	Port Function Register
00000424H	PFR4[R/W] B,H,W 00000000	PFR5[R/W] B,H,W 00000000	Reserved	PFR7[R/W] B,H,W ----0000	
00000428H	PFR8[R/W] B,H,W 00000000	PFR9[R/W] B,H,W 00000000	PFRA[R/W] B,H,W ----0000	PFRB[R/W] B,H,W 00000000	
0000042CH	PFRC[R/W] B,H,W ----0000	PFRD[R/W] B,H,W 00000000	PFRE[R/W] B,H,W 00000000	PFRF[R/W] B,H,W 00000000	
00000430H	PFRG[R/W] B,H,W ----0000	-	-	-	
00000434H to 0000043CH	-				Reserved
00000440H	ICR00[R/W] B,H,W ---11111	ICR01[R/W] B,H,W ---11111	ICR02[R/W] B,H,W ---11111	ICR03[R/W] B,H,W ---11111	Interrupt Control Unit
00000444H	ICR04[R/W] B,H,W ---11111	ICR05[R/W] B,H,W ---11111	ICR06[R/W] B,H,W ---11111	ICR07[R/W] B,H,W ---11111	
00000448H	ICR08[R/W] B,H,W ---11111	ICR09[R/W] B,H,W ---11111	ICR10[R/W] B,H,W ---11111	ICR11[R/W] B,H,W ---11111	
0000044CH	ICR12[R/W] B,H,W ---11111	ICR13[R/W] B,H,W ---11111	ICR14[R/W] B,H,W ---11111	ICR15[R/W] B,H,W ---11111	

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
00000450H	ICR16[R/W] B,H,W ---11111	ICR17[R/W] B,H,W ---11111	ICR18[R/W] B,H,W ---11111	ICR19[R/W] B,H,W ---11111	Interrupt Control Unit
00000454H	ICR20[R/W] B,H,W ---11111	ICR21[R/W] B,H,W ---11111	ICR22[R/W] B,H,W ---11111	ICR23[R/W] B,H,W ---11111	
00000458H	ICR24[R/W] B,H,W ---11111	ICR25[R/W] B,H,W ---11111	ICR26[R/W] B,H,W ---11111	ICR27[R/W] B,H,W ---11111	
0000045CH	ICR28[R/W] B,H,W ---11111	ICR29[R/W] B,H,W ---11111	ICR30[R/W] B,H,W ---11111	ICR31[R/W] B,H,W ---11111	
00000460H	ICR32[R/W] B,H,W ---11111	ICR33[R/W] B,H,W ---11111	ICR34[R/W] B,H,W ---11111	ICR35[R/W] B,H,W ---11111	
00000464H	ICR36[R/W] B,H,W ---11111	ICR37[R/W] B,H,W ---11111	ICR38[R/W] B,H,W ---11111	ICR39[R/W] B,H,W ---11111	
00000468H	ICR40[R/W] B,H,W ---11111	ICR41[R/W] B,H,W ---11111	ICR42[R/W] B,H,W ---11111	ICR43[R/W] B,H,W ---11111	
0000046CH	ICR44[R/W] B,H,W ---11111	ICR45[R/W] B,H,W ---11111	ICR46[R/W] B,H,W ---11111	ICR47[R/W] B,H,W ---11111	
00000470H to 0000047CH	-				Reserved
00000480H	RSRR [R/W] B,H,W 10000000	STCR [R/W] B,H,W 00110011	TBCR [R/W] B,H,W 00XXXX11	CTBR [W] B,H,W XXXXXXXX	Clock Control Unit
00000484H	CLKR [W] B,H,W 00000000	WPR [R/W] B,H,W XXXXXXXX	DIVR0 [R/W] B,H,W 00000011	DIVR1 [R/W] B,H,W 00000000	
00000488H	-	-	OSCCR [R/W] B X000XXX0	-	Clock Control Unit
0000048CH	Reserved				
00000490H	OSCR [R/W] B 000--001	Reserved			
00000494H to 000004ACH	-				Reserved

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
000004B0H	-	TRG2[R/W] B,H,W 00000000	-	REVC2[R/W] B,H,W 00000000	PPG2
00000B4H	PRLHG[R/W] B,H,W 00000000	PRLLG[R/W]B,H,W XXXXXXXX	PRLHH[R/W] B,H,W XXXXXXXX	PRLLH[R/W]B,H,W XXXXXXXX	
000004B8H	PRLHI[R/W]B,H,W 00000000	PRLLI[R/W]B,H,W XXXXXXXX	PRLHJ[R/W]B,H,W XXXXXXXX	PRLLJ[R/W]B,H,W XXXXXXXX	
000004BCH	PPGCG[R/W] B,H,W 0000000X	PPGCH[R/W] B,H,W 0000000X	PPGCI[R/W]B,H,W 0000000X	PPGCJ[R/W]B,H,W 0000000X	
000004C0H	PRLHK[R/W]B,H,W 00000000	PRLLK[R/W]B,H,W XXXXXXXX	PRLHL[R/W]B,H,W XXXXXXXX	PRLLL[R/W]B,H,W XXXXXXXX	
000004C4H	PRLHM[R/W] B,H,W 00000000	PRLLM[R/W]B,H,W XXXXXXXX	PRLHN[R/W] B,H,W XXXXXXXX	PRLLN[R/W]B,H,W XXXXXXXX	
000004C8H	PPGCK[R/W] B,H,W 0000000X	PPGCL[R/W] B,H,W 0000000X	PPGCM[R/W] B,H,W 0000000X	PPGCN[R/W] B,H,W 0000000X	
000004CCH	-				
000004D0H	TRG3[R/W] B,H,W 00000000	-	REVC3[R/W] B,H,W 00000000	-	PPG3
000004D4H	PRLHO[R/W] B,H,W 00000000	PRLLO[R/W]B,H,W XXXXXXXX	PRLHP[R/W]B,H,W XXXXXXXX	PRLLP[R/W]B,H,W XXXXXXXX	
000004D8H	PRLHQ[R/W] B,H,W 00000000	PRLLQ[R/W]B,H,W XXXXXXXX	PRLHR[R/W] B,H,W XXXXXXXX	PRLLR[R/W]B,H,W XXXXXXXX	
000004DCH	PPGCO[R/W] B,H,W 0000000X	PPGCP[R/W] B,H,W 0000000X	PPGCQ[R/W] B,H,W 0000000X	PPGCR[R/W] B,H,W 0000000X	
000004E0H	PRLHS[R/W]B,H,W 00000000	PRLLS[R/W]B,H,W XXXXXXXX	PRLHT[R/W]B,H,W XXXXXXXX	PRLLT[R/W]B,H,W XXXXXXXX	
000004E4H	PRLHU[R/W] B,H,W 00000000	PRLLU[R/W]B,H,W XXXXXXXX	PRLHV[R/W]B,H,W XXXXXXXX	PRLLV[R/W]B,H,W XXXXXXXX	
000004E8H	PPGCS[R/W] B,H,W 0000000X	PPGCT[R/W] B,H,W 0000000X	PPGCU[R/W] B,H,W 0000000X	PPGCV[R/W] B,H,W 0000000X	
000004ECH	-				

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
000004F0H to 000004F8H	-				Reserved
000004FCH	PSCR[W] B XXXXXXXX	-	-	-	Port Input Level Select Register
00000500H to 0000053CH	-				Reserved
00000540H	PILR0[R/W] B 00000000	PILR1[R/W] B 00000000	Reserved	Reserved	Port Input Level Select Register
00000544H	PILR4[R/W] B 00000000	PILR5[R/W] B 00000000	Reserved	-	
00000548H	-				
0000054CH	-	-	PILRE[R/W] B 00000000	Reserved	
00000550H	-				
00000554H to 0000055CH	-				Reserved
00000560H	IBCR0[R/W] B,H,W 00000000	IBSR0[R] B,H,W 00000000	ITBAH0[R/W] B,H,W ------00	ITBAL0[R/W] B,H,W 00000000	I²C0
00000564H	ITMKH0[R/W] B,H,W 00----11	ITMKL0[R/W] B,H,W 11111111	ISMK0[R/W] B,H,W 01111111	ISBA0[R/W] B,H,W -0000000	
00000568H	-	IDAR0[R/W] B,H,W 00000000	ICCR0[R/W] B,H,W -0011111	IDBL0[R/W] B,H,W -------0	
0000056CH	IBCR1[R/W] B,H,W 00000000	IBSR1[R] B,H,W 00000000	ITBAH1[R/W] B,H,W ------00	ITBAL1[R/W] B,H,W 00000000	I²C1
00000570H	ITMKH1[R/W] B,H,W 00----11	ITMKL1[R/W] B,H,W 11111111	ISMK1[R/W] B,H,W 01111111	ISBA1[R/W] B,H,W -0000000	
00000574H	-	IDAR1[R/W] B,H,W 00000000	ICCR1[R/W] B,H,W -0011111	IDBL1[R/W] B,H,W -------0	
00000578H	-				Reserved
0000057CH	Reserved	LVRC[R/W] B,H,W 00011000	Reserved	Reserved	Detection of CPU operation
00000580H to 000005FCH	-				Reserved

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
00000600H	Reserved	Reserved	EPFR2[R/W] B,H,W 00000000	EPFR3[R/W] B,H,W 00000000	I/O port
00000604H	EPFR4[R/W] B,H,W 11111111	EPFR5[R/W] B,H,W 00000000	-	EPFR7[R/W] B,H,W ----0000	
00000608H	EPFR8[R/W] B,H,W 00000000	EPFR9[R/W] B,H,W 00000000	-	-	
0000060CH	-	EPFRD[R/W] B,H,W 00000000	EPFRE[R/W] B,H,W 00000000	EPFRF[R/W] B,H,W 00000000	
00000610H	EPFRG[R/W] B,H,W ----0000	-	-	-	
00000614H to 0000063CH	-				Reserved
00000640H	ASR0 [R/W] B,H,W 00000000 00000000		ACR0 [R/W] B,H,W 1111XX00 00000000		T-unit
00000644H	ASR1 [R/W] B,H,W XXXXXXXX XXXXXXXX		ACR1 [R/W] B,H,W XXXXXXXX XXXXXXXX		
00000648H	ASR2 [R/W] B,H,W XXXXXXXX XXXXXXXX		ACR2 [R/W] B,H,W XXXXXXXX XXXXXXXX		
0000064CH	ASR3 [R/W] B,H,W XXXXXXXX XXXXXXXX		ACR3 [R/W] B,H,W XXXXXXXX XXXXXXXX		
00000650H to 0000065CH	Reserved				
00000660H	AWR0 [R/W] B,H,W 01111111 11111111		AWR1 [R/W] B,H,W XXXXXXXX XXXXXXXX		
00000664H	AWR2 [R/W] B,H,W XXXXXXXX XXXXXXXX		AWR3 [R/W] B,H,W XXXXXXXX XXXXXXXX		
00000668H to 0000067CH	Reserved				
00000680H	CSER[R/W] B,H,W XXXX0001	-	-	-	
00000684H to 000007F8H	-				Reserved
000007FCH	-	MODR *	-	-	-

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
00000800H to 00000FFCH	Reserved				
00001000H	DMASA0[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				DMAC
00001004H	DMADA0[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00001008H	DMASA1[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000100CH	DMADA1[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00001010H	DMASA2[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00001014H	DMADA2[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00001018H	DMASA3[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000101CH	DMADA3[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00001020H	DMASA4[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00001024H	DMADA4[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00001028H to 00006FFCH	Reserved				
00007000H	FLCR[R/W] 01XX1000	-	-	-	Flash I/F
00007004H	FLWC[R/W] 00000011	-	-	-	
00007008H to 0000FFFCH	Reserved				
00020000H	CTRLR0 00000000 00000001		STATR0 00000000 00000000		CAN0
00020004H	ERRCNT0 00000000 00000000		BTR0 00100011 00000001		
00020008H	INTR0 00000000 00000000		TESTR0 00000000 r0000000* (r : indication the level on the CAN bus)		
0002000CH	BRPER0 00000000 00000000		Reserved		

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
00020010H	IF1CREQ0 00000000 00000001		IF1CMSK0 00000000 00000000		CAN0
00020014H	IF1MSK20 11111111 11111111		IF1MSK10 11111111 11111111		
00020018H	IF1ARB20 00000000 00000000		IF1ARB10 00000000 00000000		
0002001CH	IF1MCTR0 00000000 00000000		-		
00020020H	IF1DTA10 00000000 00000000		IF1DTA20 00000000 00000000		
00020024H	IF1DTB10 00000000 00000000		IF1DTB20 00000000 00000000		
00020028H to 0002002CH	Reserved				
00020030H	IF1DTA20 00000000 00000000		IF1DTA10 00000000 00000000		
00020034H	IF1DTB20 00000000 00000000		IF1DTB10 00000000 00000000		
00020038H to 0002003CH	Reserved				
00020040H	IF2CREQ0 00000000 00000001		IF2CMSK0 00000000 00000000		
00020044H	IF2MSK20 00000000 00000000		IF2MSK10 00000000 00000000		
00020048H	IF2ARB20 00000000 00000000		IF2ARB10 00000000 00000000		
0002004CH	IF2MCTR0 00000000 00000000		-		
00020050H	IF2DTA10 00000000 00000000		IF2DTA20 00000000 00000000		
00020054H	IF2DTB10 00000000 00000000		IF2DTB20 00000000 00000000		
00020058H to 0002005CH	Reserved				
00020060H	IF2DTA20 00000000 00000000		IF2DTA10 00000000 00000000		
00020064H	IF2DTB20 00000000 00000000		IF2DTB10 00000000 00000000		

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
00020068H to 0002007CH	Reserved				CAN0
00020080H	Reserved		TREQR10 00000000 00000000		
00020084H to 0002008CH	Reserved				
00020090H	Reserved		NEWDT10 00000000 00000000		
00020094H to 0002009CH	Reserved				
000200A0H	Reserved		INTPEND10 00000000 00000000		
000200A4H to 000200ACH	Reserved				
000200B0H	Reserved		MESVAL10 00000000 00000000		
000200B4H to 000200BCH	Reserved				
00020100H	CTRLR1 00000000 00000001		STATR1 00000000 00000000		CAN1
00020104H	ERRCNT1 00000000 00000000		BTR1 00100011 00000001		
00020108H	INTR1 00000000 00000000		TESTR1 00000000 r0000000*		
0002010CH	BRPER1 00000000 00000000		Reserved		
00020110H	IF1CREQ1 00000000 00000001		IF1CMSK1 00000000 00000000		
00020114H	IF1MSK21 11111111 11111111		IF1MSK11 11111111 11111111		
00020118H	IF1ARB21 00000000 00000000		IF1ARB11 00000000 00000000		

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
0002011C$_H$	IF1MCTR1 00000000 00000000		-		CAN1
00020120$_H$	IF1DTA11 00000000 00000000		IF1DTA21 00000000 00000000		
00020124$_H$	IF1DTB11 00000000 00000000		IF1DTB21 00000000 00000000		
00020128$_H$ to 0002012C$_H$	Reserved				
00020130$_H$	IF1DTA21 00000000 00000000		IF1DTA11 00000000 00000000		
00020134$_H$	IF1DTB21 00000000 00000000		IF1DTB11 00000000 00000000		
00020138$_H$ to 0002013C$_H$	Reserved				
00020140$_H$	IF2CREQ1 00000000 00000001		IF2CMSK1 00000000 00000000		
00020144$_H$	IF2MSK21 00000000 00000000		IF2MSK11 00000000 00000000		
00020148$_H$	IF2ARB21 00000000 00000000		IF2ARB11 00000000 00000000		
0002014C$_H$	IF2MCTR1 00000000 00000000		-		
00020150$_H$	IF2DTA11 00000000 00000000		IF2DTA21 00000000 00000000		
00020154$_H$	IF2DTB11 00000000 00000000		IF2DTB21 00000000 00000000		
00020158$_H$ to 0002015C$_H$	Reserved				
00020160$_H$	IF2DTA21 00000000 00000000		IF2DTA11 00000000 00000000		
00020164$_H$	IF2DTB21 00000000 00000000		IF2DTB11 00000000 00000000		
00020168$_H$ to 0002017C$_H$	Reserved				
00020180$_H$	Reserved		TREQR11 00000000 00000000		

(Continued)

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
00020184H to 0002018CH	Reserved				CAN1
00020190H	Reserved		NEWDT11 00000000 00000000		
00020194H to 0002019CH	Reserved				
000201A0H	Reserved		INTPEND11 00000000 00000000		
000201A4H to 000201ACH	Reserved				
000201B0H	Reserved		MESVAL11 00000000 00000000		
000201B4H to 000201BCH	Reserved				

* : The lower 16 bits (DTC [15 : 0]) of DMCA0 to DMCA4 cannot be accessed in bytes.

Notes : • Do not perform read modify write instructions to a register including write-on-bit.
• The data in the area reserved or - is undefined.

■ VECTOR TABLE

Interrupt source	Interrupt number		Interrupt level	Offset	TBR default address	DMA start source
	Decimal	Hexa-decimal				
Reset	0	00	—	3FC$_H$	000FFFFC$_H$	—
Mode vector	1	01	—	3F8$_H$	000FFFF8$_H$	—
System reserved	2	02	—	3F4$_H$	000FFFF4$_H$	—
System reserved	3	03	—	3F0$_H$	000FFFF0$_H$	—
System reserved	4	04	—	3EC$_H$	000FFFEC$_H$	—
System reserved	5	05	—	3E8$_H$	000FFFE8$_H$	—
System reserved	6	06	—	3E4$_H$	000FFFE4$_H$	—
Coprocessor absent trap	7	07	—	3E0$_H$	000FFFE0$_H$	—
Coprocessor error trap	8	08	—	3DC$_H$	000FFFDC$_H$	—
INTE instruction	9	09	—	3D8$_H$	000FFFD8$_H$	—
System reserved	10	0A	—	3D4$_H$	000FFFD4$_H$	—
System reserved	11	0B	—	3D0$_H$	000FFFD0$_H$	—
Step trace trap	12	0C	—	3CC$_H$	000FFFCC$_H$	—
NMI request (ICE)	13	0D	—	3C8$_H$	000FFFC8$_H$	—
Undefined instruction exception	14	0E	—	3C4$_H$	000FFFC4$_H$	—
NMI instruction	15	0F	0F$_H$ Fixed	3C0$_H$	000FFFC0$_H$	—
External interrupt 0/1/2/6/7	16	10	ICR00	3BC$_H$	000FFFBC$_H$	—
External interrupt 3	17	11	ICR01	3B8$_H$	000FFFB8$_H$	6
External interrupt 4	18	12	ICR02	3B4$_H$	000FFFB4$_H$	7
External interrupt 5	19	13	ICR03	3B0$_H$	000FFFB0$_H$	—
PPG0H/0L/8H/8L	20	14	ICR04	3AC$_H$	000FFFAC$_H$	—
PPG2H/2L/9H/9L	21	15	ICR05	3A8$_H$	000FFFA8$_H$	—
PPG4H/4L/10H/10L	22	16	ICR06	3A4$_H$	000FFFA4$_H$	—
PPG6H/6L/11H/11L	23	17	ICR07	3A0$_H$	000FFFA0$_H$	—
Reload timer 0	24	18	ICR08	39C$_H$	000FFF9C$_H$	8
Reload timer 1	25	19	ICR09	398$_H$	000FFF98$_H$	9
Reload timer 2	26	1A	ICR10	394$_H$	000FFF94$_H$	10
LIN-UART0 (Reception)	27	1B	ICR11	390$_H$	000FFF90$_H$	—
LIN-UART0 (Transmission)	28	1C	ICR12	38C$_H$	000FFF8C$_H$	—
LIN-UART1 (Reception)	29	1D	ICR13	388$_H$	000FFF88$_H$	1
LIN-UART1 (Transmission)	30	1E	ICR14	384$_H$	000FFF84$_H$	4
LIN-UART2 (Reception)	31	1F	ICR15	380$_H$	000FFF80$_H$	2
LIN-UART2 (Transmission)	32	20	ICR16	37C$_H$	000FFF7C$_H$	5
LIN-UART3 (Reception)	33	21	ICR17	378$_H$	000FFF78$_H$	—
LIN-UART3 (Transmission)	34	22	ICR18	374$_H$	000FFF74$_H$	—

(Continued)

(Continued)

Interrupt source	Interrupt number		Interrupt level	Offset	TBR default address	DMA start source
	Decimal	Hexa-decimal				
CAN0	35	23	ICR19	370H	000FFF70H	—
CAN1	36	24	ICR20	36CH	000FFF6CH	—
PPG12H/12L/I²C0	37	25	ICR21	368H	000FFF68H	—
PPG13H/13L	38	26	ICR22	364H	000FFF64H	—
PPG14H/14L/I²C1	39	27	ICR23	360H	000FFF60H	—
PWC (Measurement completed)	40	28	ICR24	35CH	000FFF5CH	—
PWC (Overflow)	41	29	ICR25	358H	000FFF58H	—
DMAC	42	2A	ICR26	354H	000FFF54H	—
A/D converter	43	2B	ICR27	350H	000FFF50H	14
Real-time clock	44	2C	ICR28	34CH	000FFF4CH	—
PPG15H/15L	45	2D	ICR29	348H	000FFF48H	—
Main oscillation stabilization wait timer	46	2E	ICR30	344H	000FFF44H	—
Timebase timer overflow	47	2F	ICR31	340H	000FFF40H	—
PPG1H/1L	48	30	ICR32	33CH	000FFF3CH	11
PPG3H/3L	49	31	ICR33	338H	000FFF38H	12
PPG5H/5L	50	32	ICR34	334H	000FFF34H	13
PPG7H/7L	51	33	ICR35	330H	000FFF30H	3
16-bit free-run timer 0	52	34	ICR36	32CH	000FFF2CH	—
16-bit free-run timer 1	53	35	ICR37	328H	000FFF28H	—
ICU0	54	36	ICR38	324H	000FFF24H	—
ICU1	55	37	ICR39	320H	000FFF20H	—
ICU2	56	38	ICR40	31CH	000FFF1CH	—
ICU3	57	39	ICR41	318H	000FFF18H	—
OCU0	58	3A	ICR42	314H	000FFF14H	—
OCU1	59	3B	ICR43	310H	000FFF10H	—
Sound generator 0	60	3C	ICR44	30CH	000FFF0CH	—
Sound generator 1	61	3D	ICR45	308H	000FFF08H	—
Sound generator 2	62	3E	ICR46	304H	000FFF04H	—
Delay interrupt	63	3F	ICR47	300H	000FFF00H	—
System reserved	64	40	—	2FCH	000FFEFCH	—
System reserved	65	41	—	2F8H	000FFEF8H	—
System reserved	66 to 79	42 to 4F	—	2F4H to 2C0H	000FFEF4H to 000FFEC0H	—
INT instruction	80 to 255	50 to FF	—	2BCH to 000H	000FFEBCH to 000FFC00H	—

■ TABLE OF PIN STATUS IN EACH MODE

• **Single chip mode**

Pin Name	Function name	Initial value		In SLEEP State	In STOP State		Remarks
		INITX=L	INITX=H		HIZ=0	HIZ=1	
INITX	INIT	Input permitted	Input permitted	Input permitted	Input permitted		
X0	Main clock				Hi-Z or Input permitted		
X1					"H" output or input permitted		
X0A	Sub clock				Hi-Z or input permitted		
X1A					"H" output or input permitted		
MD0	Mode				Input permitted		
MD1							
MD2							
P00	SEG24	Output Hi-Z Input cut-off	Output Hi-Z Input permitted	Previous state held	Previous state held	Output Hi-Z Input cut-off	When LCD is used, output operation or output retention for both SLEEP/STOP
P01	SEG25						
P02	SEG26						
P03	SEG27						
P04	SEG28						
P05	SEG29						
P06	SEG30						
P07	SEG31/ATGX						
P10	SEG16	Output Hi-Z Input cut-off	Output Hi-Z Input permitted	Previous state held	Previous state held	Output Hi-Z Input cut-off	When LCD is used, output operation or output retention for both SLEEP/STOP
P11	SEG17						
P12	SEG18						
P13	SEG19						
P14	SEG20						
P15	SEG21						
P16	SEG22						
P17	SEG23						

(Continued)

Pin Name	Function name	Initial value		In SLEEP State	In STOP State		Remarks
		INITX=L	INITX=H		HIZ=0	HIZ=1	
P20	SEG0	Output Hi-Z Input cut-off	Output Hi-Z Input permitted	Previous state held	Previous state held	Output Hi-Z Input cut-off	When LCD is used, output operation or output retention for both SLEEP/STOP
P21	SEG1						
P22	SEG2						
P23	SEG3						
P24	SEG4						
P25	SEG5						
P26	SEG6						
P27	SEG7						
P30	SEG8	Output Hi-Z Input cut-off	Output Hi-Z Input permitted	Previous state held	Previous state held	Output Hi-Z Input cut-off	When LCD is used, output operation or output retention for both SLEEP/STOP
P31	SEG9						
P32	SEG10						
P33	SEG11						
P34	SEG12						
P35	SEG13						
P36	SEG14						
P37	SEG15						
P40	SIN0/INT0	Output Hi-Z Input permitted	Output Hi-Z Input permitted	Previous state held	Previous state held	Output Hi-Z Input cut-off	Input of external interrupt is enabled by setting PFR
P41	SOT0						
P42	SCK0						
P43	SIN3/INT1						
P44	SOT3						
P45	SCK3						
P46	—						
P47	—						
P50	SIN4/CK0	Output Hi-Z Input permitted	Output Hi-Z Input permitted	Previous state held	Previous state held	Output Hi-Z Input cut-off	
P51	SOT4						
P52	SCK4						
P53	SIN5/CK1						
P54	SOT5						
P55	SCK5						
P56	OUT0						
P57	OUT1						

(Continued)

Pin Name	Function name	Initial value		In SLEEP State	In STOP State		Remarks
		INITX=L	INITX=H		HIZ=0	HIZ=1	
P60	AN0	Output Hi-Z Input cut-off	Output Hi-Z Input cut-off	Previous state held	Previous state held	Output Hi-Z Input cut-off	
P61	AN1						
P62	AN2						
P63	AN3						
P64	AN4						
P65	AN5						
P66	AN6						
P67	AN7						
P70	INT60/RX0	Output Hi-Z Input permitted	Input permitted	Previous state held	Previous state held	Output Hi-Z Input cut-off	Input of external interrupt is enabled by setting PFR
P71	TX0						
P72	INT7/RX1						
P73	TX1						
P80	AN16	Output Hi-Z Input cut-off	Output Hi-Z Input cut-off	Previous state held	Previous state held	Output Hi-Z Input cut-off	
P81	AN17						
P82	AN18						
P83	AN19						
P84	AN20/INT2						
P85	AN21/INT3						
P86	AN22/INT4						
P87	AN23/INT5						
P90	DA0	Output Hi-Z Input permitted	Output Hi-Z Input permitted	Previous state held	Previous state held	Output Hi-Z Input cut-off	When DA is used, output retention
P91	DA1						
P92	SGA0						
P93	SGO0						
P94	SGA1						
P95	SGO1						
P96	SGA2						
P97	SGO2						
PA0	PWM1P3	Output Hi-Z Input permitted	Output Hi-Z Input permitted	Previous state held	Previous state held	Output Hi-Z Input cut-off	
PA1	PWM1M3						
PA2	PWM2P3						
PA3	PWM2M3						

(Continued)

Pin Name	Function name	Initial value		In SLEEP State	In STOP State		Remarks
		INITX=L	INITX=H		HIZ=0	HIZ=1	
PB0	PPG8H	Output Hi-Z Input permitted	Output Hi-Z Input permitted	Previous state held	Previous state held	Output Hi-Z Input cut-off	
PB1	PPG9H						
PB2	PPG10H						
PB3	PPG11H						
PB4	PWM1P1						
PB5	PWM1M1						
PB6	PWM2P1						
PB7	PWM2M1						
PC0	PWM1P0	Output Hi-Z Input permitted	Output Hi-Z Input permitted	Previous state held	Previous state held	Output Hi-Z Input cut-off	
PC1	PWM1M0						
PC2	PWM2P0						
PC3	PWM2M0						
PD0	TIN0/IN0/PWC0/INT2/V0	Input permitted	Input permitted	Previous state held	Previous state held	Output Hi-Z Input cut-off	Input of external interrupt is enabled by setting PFR When LCD is used, output operation or output retention for both SLEEP/STOP
PD1	TIN1/IN1/V1						
PD2	TIN2/IN2/V2						
PD3	IN3/V3						
PD4	COM0/PPG1H	"L" output Input permitted	"L" output Input permitted	Previous state held			
PD5	COM1/PPG3H						
PD6	COM2/PPG5H						
PD7	COM3/PPG7H						
PE0	PWM1P2	Output Hi-Z Input permitted	Output Hi-Z Input permitted	Previous state held	Previous state held	Output Hi-Z Input cut-off	
PE1	PWM1M2						
PE2	PWM2P2						
PE3	PWM2M2						
PE4	PPG12H/SDA0						
PE5	PPG13H/SCL0						
PE6	PPG14H/SDA1						
PE7	PPG15H/SCL1						

(Continued)

(Continued)

Pin Name	Function name	Initial value		In SLEEP State	In STOP State		Remarks
		INITX=L	INITX=H		HIZ=0	HIZ=1	
PF0	AN8	Output Hi-Z Input cut-off	Output Hi-Z Input cut-off	Previous state held	Previous state held	Output Hi-Z Input cut-off	
PF1	AN9						
PF2	AN10						
PF3	AN11						
PF4	AN12						
PF5	AN13						
PF6	AN14						
PF7	AN15						
PG0	PPG0H	Output Hi-Z Input permitted	Output Hi-Z Input permitted	Previous state held	Previous state held	Output Hi-Z Input cut-off	
PG1	TOT0/PPG2H						
PG2	TOT1/PPG4H						
PG3	TOT2/PPG6H						

• **External bus mode (8-bit)**

Pin Name	Function name	Initial value		In SLEEP State	In STOP State		Remarks
		INITX=L	INITX=H		HIZ=0	HIZ=1	
INITX	INIT	Input permitted	Input permitted	Input permitted	Input permitted		
X0	Main clock				Hi-Z or Input permitted		
X1					"H" output or input permitted		
X0A	Sub clock				Hi-Z or Input permitted		
X1A					"H" output or input permitted		
MD0	Mode				Input permitted		
MD1							
MD2							
P00	SEG24	Output Hi-Z Input cut-off	Output Hi-Z Input permitted	Previous state held	Previous state held	Output Hi-Z Input cut-off	When LCD is used, output operation or output retention for both SLEEP/STOP
P01	SEG25						
P02	SEG26						
P03	SEG27						
P04	SEG28						
P05	SEG29						
P06	SEG30						
P07	SEG31/ATGX						
P10	D08	Output Hi-Z Input cut-off	Output Hi-Z Input permitted	Hi-Z	Hi-Z	Output Hi-Z Input cut-off	No port function
P11	D09						
P12	D10						
P13	D11						
P14	D12						
P15	D13						
P16	D14						
P17	D15						
P20	A00	Output Hi-Z Input cut-off	Output Hi-Z Input permitted	Address output	Address output	Output Hi-Z Input cut-off	No port function
P21	A01						
P22	A02						
P23	A03						
P24	A04						
P25	A05						
P26	A06						
P27	A07						

(Continued)

(Continued)

Pin Name	Function name	Initial value		In SLEEP State	In STOP State		Remarks
		INITX=L	INITX=H		HIZ=0	HIZ=1	
P30	A08	Output Hi-Z Input cut-off	Output Hi-Z Input permitted	Address output	Address output	Output Hi-Z Input cut-off	No port function
P31	A09						
P32	A10						
P33	A11						
P34	A12						
P35	A13						
P36	A14						
P37	A15						
P40	SIN0/INT0	Output Hi-Z Input permitted	Output Hi-Z Input permitted	Previous state held	Previous state held	Output Hi-Z Input cut-off	Input of external interrupt is enabled by setting PFR When external bus signal is used, "H" output/clock output for SLEEP/STOP (Hi-Z=0)
P41	SOT0						
P42	SCK0						
P43	SIN3/INT1						
P44	SOT3						
P45	SCK3						
P46	ASX		"H" output				
P47	SYSCLK		Clock output				
P50	SIN4/CK0/CS0X	Output Hi-Z Input permitted	Output Hi-Z Input permitted	Previous state held	Previous state held	Output Hi-Z Input cut-off	When external bus signal is used, "H" output for SLEEP/ STOP (Hi-Z=0)
P51	SOT4/CS1X						
P52	SCK4/CS2X						
P53	SIN5/CK1/CS3X						
P54	SOT5/RDX						
P55	SCK5/WR0X						
P56	OUT0						
P57	OUT1/RDY		Input permitted				
P60 to PG3	It is the same as the single chip.						

• **External bus mode (16-bit)**

Pin Name	Function name	Initial value		In SLEEP State	In STOP State		Remarks
		INITX=L	INITX=H		HIZ=0	HIZ=1	
INITX	INIT	Input permitted	Input permitted	Input permitted	Input permitted		
X0	Main clock				Hi-Z or Input permitted		
X1					"H" output or input permitted		
X0A	Sub clock				Hi-Z or Input permitted		
X1A					"H" output or input permitted		
MD0	Mode				Input permitted		
MD1							
MD2							
P00	D00	Output Hi-Z Input cut-off	Output Hi-Z Input permitted	Hi-Z	Hi-Z	Output Hi-Z Input cut-off	No port function
P01	D01						
P02	D02						
P03	D03						
P04	D04						
P05	D05						
P06	D06						
P07	D07						
P10	D08	Output Hi-Z Input cut-off	Output Hi-Z Input permitted	Hi-Z	Hi-Z	Output Hi-Z Input cut-off	No port function
P11	D09						
P12	D10						
P13	D11						
P14	D12						
P15	D13						
P16	D14						
P17	D15						
P20	A00	Output Hi-Z Input cut-off	Output Hi-Z Input permitted	Address output	Address output	Output Hi-Z Input cut-off	No port function
P21	A01						
P22	A02						
P23	A03						
P24	A04						
P25	A05						
P26	A06						
P27	A07						

(Continued)

(Continued)

Pin Name	Function name	Initial value		In SLEEP State	In STOP State		Remarks
		INITX=L	INITX=H		HIZ=0	HIZ=1	
P30	A08	Output Hi-Z Input cut-off	Output Hi-Z Input permitted	Address output	Address output	Output Hi-Z Input cut-off	No port function
P31	A09						
P32	A10						
P33	A11						
P34	A12						
P35	A13						
P36	A14						
P37	A15						
P40	SIN0/INT0	Output Hi-Z Input permitted	Output Hi-Z Input permitted	Previous state held	Previous state held	Output Hi-Z Input cut-off	Input of external interrupt is enabled by setting PFR When external bus signal is used, "H" output/clock output for SLEEP/STOP (Hi-Z=0)
P41	SOT0						
P42	SCK0						
P43	SIN3/INT1						
P44	SOT3						
P45	SCK3						
P46	ASX		"H" output				
P47	SYSCLK		Clock output				
P50	SIN4/CK0/CS0X	Output Hi-Z Input permitted	Output Hi-Z Input permitted	Previous state held	Previous state held	Output Hi-Z Input cut-off	When external bus signal is used, "H" output for SLEEP/ STOP (Hi-Z=0)
P51	SOT4/CS1X						
P52	SCK4/CS2X						
P53	SIN5/CK1/CS3X						
P54	SOT5/RDX						
P55	SCK5/WR0X						
P56	OUT0/WR1X						
P57	OUT1/RDY		Input permitted				
P60 to PG3	It is the same as the single chip.						

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	V_{CC}	V_{SS} – 0.3	V_{SS} + 6.0	V	
	AV_{CC}	V_{SS} – 0.3	V_{SS} + 6.0	V	$AV_{CC} = V_{CC}$*2
	V_{AVRH}	V_{SS} – 0.3	V_{SS} + 6.0	V	$AV_{CC} \geq V_{AVRH}$
	DV_{CC}	V_{SS} – 0.3	V_{SS} + 6.0	V	$DV_{CC} = V_{CC}$*2
Input voltage*1	V_I	V_{SS} – 0.3	V_{CC} + 6.0	V	*9
Output voltage*1	V_O	V_{SS} – 0.3	V_{CC} + 6.0	V	*9
"L" level maximum output current*3	I_{OL1}	—	15	mA	*5
	I_{OL2}	—	40	mA	*6
"L" level average output current*4	I_{OLAV1}	—	4	mA	*5
	I_{OLAV2}	—	30	mA	*6
"L" level total maximum output current	ΣI_{OL1}	—	120	mA	*5
	ΣI_{OL2}	—	330	mA	*6
"L" level total average output current	ΣI_{OLAV1}	—	50	mA	*5
	ΣI_{OLAV2}	—	160	mA	*6
"H" level maximum output current	I_{OH1}*3	—	–15	mA	*5
	I_{OH2}*3	—	–40	mA	*6
"H" level average output current	I_{OHAV1}*4	—	–4	mA	*5
	I_{OHAV2}*4	—	–30	mA	*6
"H" level total maximum output current	ΣI_{OH1}	—	–120	mA	*5
	ΣI_{OH2}	—	–330	mA	*6
"H" level total average output current	ΣI_{OHAV1}*7	—	–50	mA	*5
	ΣI_{OHAV2}*7	—	–160	mA	*6
Power consumption	P_D	—	660	mW	
Operating temperature	T_A	–40	+105	°C	In single chip operation
		–40	+85	°C	In external bus operation
Storage temperature	Tstg	–55	+150	°C	
+B input standard (Maximum clamp current)	I_{CLAMP}	–2	+2	mA	Except dedicated input pins, (PD3 to PD0) and D/AC output pins (P91, P90) *8
+B input standard (Total maximum clamp current)	ΣI_{CLAMP}	–20	+20	mA	

(Continued)

(Continued)

*1 : The parameter is based on V_{SS} = AV_{SS} = DV_{SS} = 0.0 V.

*2 : Note that AV_{CC} and DV_{CC} should not exceed V_{CC} upon power-on and under other circumstances.

*3 : The maximum output current defines the peak current value of each of the corresponding pins.

*4 : The average output current defines the average value of the current (100 ms) which passes through each of the corresponding pins. The average value represents a value calculated by multiplying the operating current by the operating rate.

*5 : Output other than PA0 to PA3 pins, PB4 to PB7 pins, PC0 to PC3 pins, and PE0 to PE3 pins.

*6 : (PA0 to PA3, PE0 to PE3) + (PB4 to PB7, PC0 to PC3) .
The stepping motor controller pins are divided into two groups (8 pins each) and the value is calculated as the total current per group.

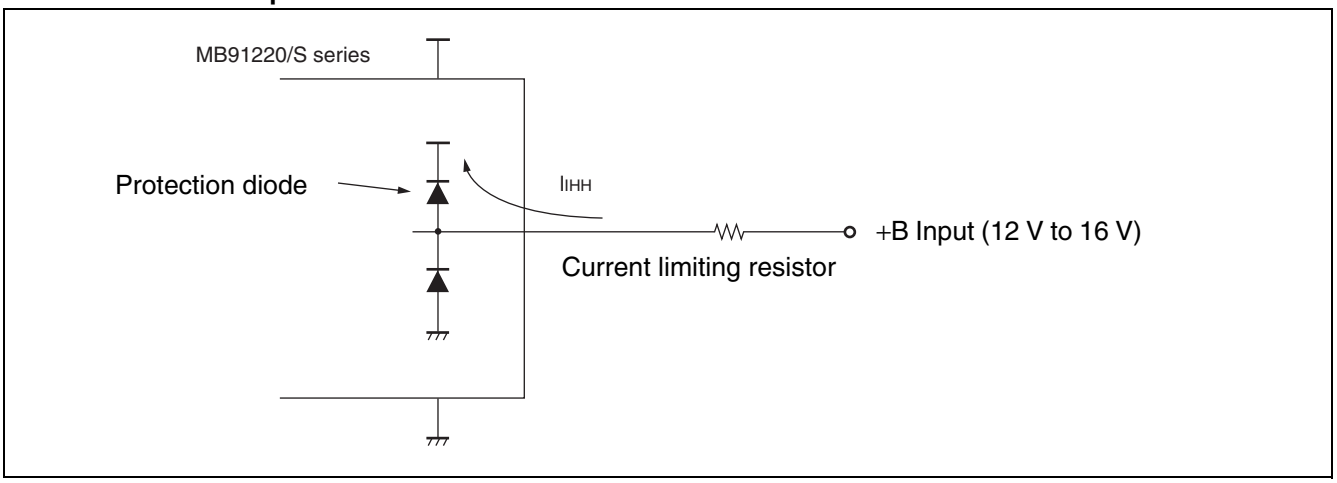
*7 : The total average output current defines the average value of the current (100 ms) which passes through all the corresponding pins. The average value represents a value calculated by multiplying the operating current by the operating rate.

*8 : +B input standard defines the current value for each of the corresponding pins.

*9 : V_I and V_O should not exceed V_{CC} + 0.3 V. However, if the maximum current to/from an input is limited by some means with external components, when the +B input-enabled pin is used the I_{CLAMP} rating supersedes the V_I rating.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

Recommended example circuit



WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

2. Recommended Operating Conditions

(V_{SS} = DV_{SS} = AV_{SS} = 0.0 V)

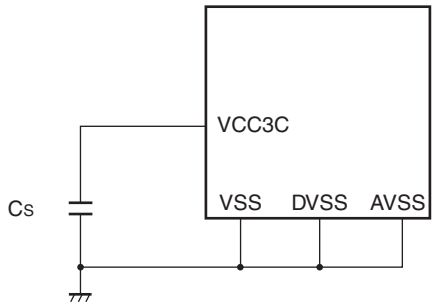
Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage	V_{CC} AV_{CC} DV_{CC}	4.5	5.5	V	Recommended guaranteed operating range
		3.5	5.5	V	Guaranteed operating range*1
		2.0	5.5	V	Guaranteed operating range for holding stop operation status*2 (MB91F223/S)
Smoothing capacitor*3	C_S	1		µF	Use a ceramic capacitor or a capacitor with similar frequency characteristics.
Operating temperature	T_A	–40	+105	°C	In single chip operation
		–40	+85	°C	In external bus operation

*1 : Exclusive of A/D and D/A operation

*2 : Internal voltage held in RAM : 1.8 V (Min) /3.6 V (Max)

*3 : For how to connect the smoothing capacitor C_S, refer to the diagram below.

• C Pin Connection Diagram



< + B input (12 V to 16 V) conditions>

- Do not connect +B potential directly to a microcontroller pin.
- Always connect a resistor between the microcontroller pin and +B signal to limit the current.

  I_{IHH} = 2 mA per pin (Max.) [In the steady state and transient state between power-on and power-off, etc.]

  It can be connected to any general-purpose input port except the output pin for LCDC.
- The protection diode in the microcontroller turns the potential upon +B input between the limiting resistor and microcontroller pin into "V_{CC} + protection diode ON voltage". Configure the circuit so that these are not interfered and the potential is not exceeded.

3. DC Specifications

(T_A : − 40 °C to + 105 °C ;Vcc = 5.0 V ±10%, V_{SS} = DV_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	V_{IHS}	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P73, P80 to P87, P90 to P97, PA0 to PA3, PB0 to PB7, PC0 to PC3, PD0 to PD7, PE0 to PE7, PF0 to PF7, PG0 to PG3	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	Automotive level input pins*1
	V_{IH}	P40, P43, P50, P53 PE4 to PE7	—	0.7 V_{CC}	—	V_{CC} + 0.3	V	CMOS input pins*2
	V_{IHT}	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P57, P60 to P67, PF0 to PF7	—	2.0	—	V_{CC} + 0.3	V	TTL input pins*4
	V_{IHM}	MD0 to MD2	—	V_{CC} − 0.3	—	V_{CC} + 0.3	V	MD pins*3
	V_{IHX}	X0, X1, X0A, X1A, INITX	—	0.8 V_{CC}	—	—	V	
"L" level input voltage	V_{ILS}	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P73, P80 to P87, P90 to P97, PA0 to PA3, PB0 to PB7, PC0 to PC3, PD0 to PD7, PE0 to PE7, PF0 to PF7, PG0 to PG3	—	V_{SS} − 0.3	—	0.5 V_{CC}	V	Automotive level input pins*1
	V_{IL}	P40, P43, P50, P53, PE4 to PE7	—	V_{SS} − 0.3	—	0.3 V_{CC}	V	CMOS hysteresis input pins*2
	V_{ILT}	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P57, P60 to P67, PF0 to PF7	—	V_{SS} − 0.3	—	0.8	V	TTL input pins*4
	V_{ILM}	MD0 to MD2	—	V_{SS} − 0.3	—	Vss + 0.3	V	MD pins*3
	V_{ILX}	X0, X1, X0A, X1A, INITX	—	—	—	0.2 V_{CC}	V	

(Continued)

(T_A : − 40 °C to + 105 °C; Vcc = 5.0 V ±10%, V_{SS} = DV_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current*5	I_{CC}	VCC	Operating frequency : F_{CP} = 32 MHz in main mode	—	85	105	mA	Under normal operation
				—	135	155	mA	In Flash-Write mode
	I_{CCS}		Operating frequency : F_{CP} = 32 MHz in main sleep mode	—	40	70	mA	
	I_{CCL}		Operating frequency : F_{CP} = 32 kHz, T_A = +25 °C in sub mode	—	200	450	µA	main oscillation/ PLL stops*6
	I_{CCLS}		Operating frequency : F_{CP} = 32 kHz, T_A = +25 °C, Vcc = 5V in sub sleep mode	—	180	400	µA	main oscillation/ PLL stops*6
	I_{CCH}		T_A = +25 °C, Vcc = 5V in stop mode (oscillation stopped)	—	10	150	µA	main clock/PLL/ sub-oscillation halted*7
	I_{CTS4M}		T_A = +25 °C, Vcc = 5V in stop mode (RTC in use*8)	—	330	500	µA	PLL/ sub-oscillation halted*7
	I_{CTS32K}		Sub clock frequency : F_{CP} = 32 kHz, T_A = +25 °C, Vcc = 5V in stop mode (Real Time Clock Operation*8)	—	40	180	µA	main oscillation/ PLL stops*6
Input leak current	I_{IL}	All input pins	V_{CC} = DV_{CC} = AV_{CC} = 5.5 V V_{SS} < V_I < V_{CC}	–5	—	+5	µA	
Input capacity 1	C_{IN1}	Other than VCC, VSS, DVCC, DVSS, AVCC, AVSS, PA0 to PA3, PB4 to PB7, PC0 to PC3, PE0 to PE3	—	—	5	15	pF	
Input capacity 2	C_{IN2}	PA0 to PA3, PB4 to PB7, PC0 to PC3, PE0 to PE3	—	—	15	45	pF	
Pull-up resistance	R_{UP}	INITX	—	25	50	100	kΩ	

(Continued)

(T_A : − 40 °C to + 105 °C; Vcc = 5.0 V ±10%, V_{SS} = DV_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Output “H” voltage 1	V_{OH1}	Other than PA0 to PA3, PB4 to PB7, PC0 to PC3, PE0 to PE3	Vcc = 4.5 V I_{OH} = −4.0 mA	V_{CC} − 0.5	—	—	V	
Output “H” voltage 2	V_{OH2}	PA0 to PA3, PB4 to PB7, PC0 to PC3, PE0 to PE3	Vcc = 4.5 V I_{OH} = −30.0 mA	V_{CC} − 0.5	—	—	V	
Output “L” voltage 1	V_{OL1}	Other than PA0 to PA3, PB4 to PB7, PC0 to PC3, PE0 to PE3	Vcc = 4.5 V I_{OL} = 4.0 mA	—	—	0.4	V	
Output “L” voltage 2	V_{OL2}	PA0 to PA3, PB4 to PB7, PC0 to PC3, PE0 to PE3	Vcc = 4.5 V I_{OL} = 30.0 mA	—	—	0.55	V	
High current output Drive capacity Phase-to-phase deviation 1	ΔV_{OH2}	PWM1Pn, PWM1Mn, PWM2Pn, PWM2Mn, n = 0 to 3	Vcc = 4.5 V I_{OH} = 30.0 mA Maximum deviation of V_{OH2}	0	—	90	mV	*9
High current output Drive capacity Phase-to-phase deviation 2	ΔV_{OL2}	PWM1Pn, PWM1Mn, PWM2Pn, PWM2Mn, n = 0 to 3	Vcc = 4.5 V I_{OL} = 30.0 mA Maximum deviation of V_{OL2}	0	—	90	mV	*9
COM0 to COM3 Output impedance	R_{VCOM}	COM0 to COM3	—	—	—	4.5	kΩ	
SEG00 to SEG31 Output impedance	R_{VSEG}	SEG0 to SEG31	—	—	—	30	kΩ	
LCDC leak current	I_{LCDC}	COM0 to COM3, SEG0 to SEG31	T_A = +25 °C	−0.5	—	+0.5	µA	

*1 : All input pins except X0, X1, X0A, X1A, MD0, MD1, MD2 and INITX pins

*2 : CMOS input can be switched by the SIN of the LIN-UART and I²C input pin and switched by the input level selection register (PILR) .

*3 : MD0, MD1, MD2

*4 : TTL input can be selected by the external bus input pins and input pin only in the parallel writer mode. The external bus input pins (P00 to P17 and P57) can be switched by the input level selection register (PILR) .

*5 : They represent current values used when supplying power to the external clock from pin X1.

(Continued)

(Continued)

*6 : Before switching from the main clock operation mode to the sub clock operation (operation in sub RUN, sub SLEEP, and sub RTC) mode, set the main oscillation stop bit (OSCDS1) in the oscillation control register (OSCCR) to "1" and the clock source to half of the source oscillation input, and then stop the PLL.

*7 : Before switching from the main clock operation mode to the stop mode, set the clock source to half of the source oscillation input , stop the PLL, set the OSDC1 bit in the standby control register (STCR) to "1". However, if using the main clock RTC operation , set the clock source to half of the source oscillation input, stop the PLL, and then set each clock of the CPU clock (CLKB) , peripheral clock (CLKP) , and external interface clock (CLKT) to the division ratio of 8 or more using the base clock divide setting registers 0 and 1 (DIVR0 and 1) before switching to the stop mode.

*8 : The real time clock can be operated only in the 4 MHz main clock oscillation or 32 kHz sub clock oscillation.

*9 : Defined by the maximum deviation of V_{OH2}/V_{OL2} of each pin, when PWM1P0, PWM1M0, PWM2P0 and PWM2M0 in ch.0 are simultaneously turned on. Other channels are applied in the same condition.

4. Flash Memory Write/Erase Characteristics

Parameter	Condition	Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time	T_A = +25 °C, Vcc = 5.0 V	—	1	15	s	Exclusive of internal write time prior to erase
Chip erase time	T_A = +25 °C, Vcc = 5.0 V	—	5	—	s	Exclusive of internal write time prior to erase
Halfword write time	T_A = +25 °C, Vcc = 5.0 V	—	16	3600	µs	Exclusive of overhead time at system level
Chip write time	T_A = +25 °C, Vcc = 5.0 V	—	2.1	—	s	Exclusive of overhead time at system level
Erase/write cycle	—	10000	—	—	cycle	
Flash memory data retain time	T_A = +85 °C (average)	10	—	—	year	*

* : This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into average temperature at + 85 °C) .

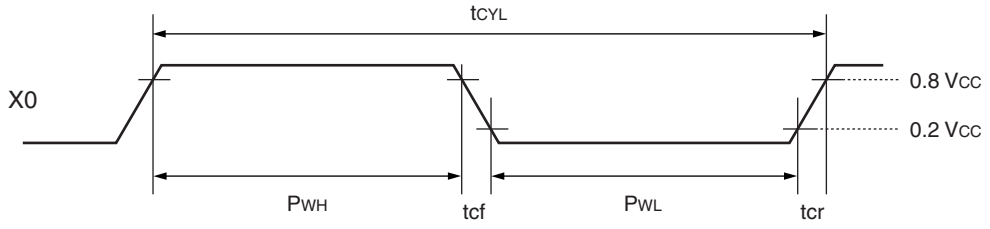
5. AC Specifications

(1) Clock timing

(T_A : − 40 °C to + 105 °C; Vcc = 5.0 V ±10%, V_{SS} = DV_{SS} = AV_{SS} = 0.0 V)

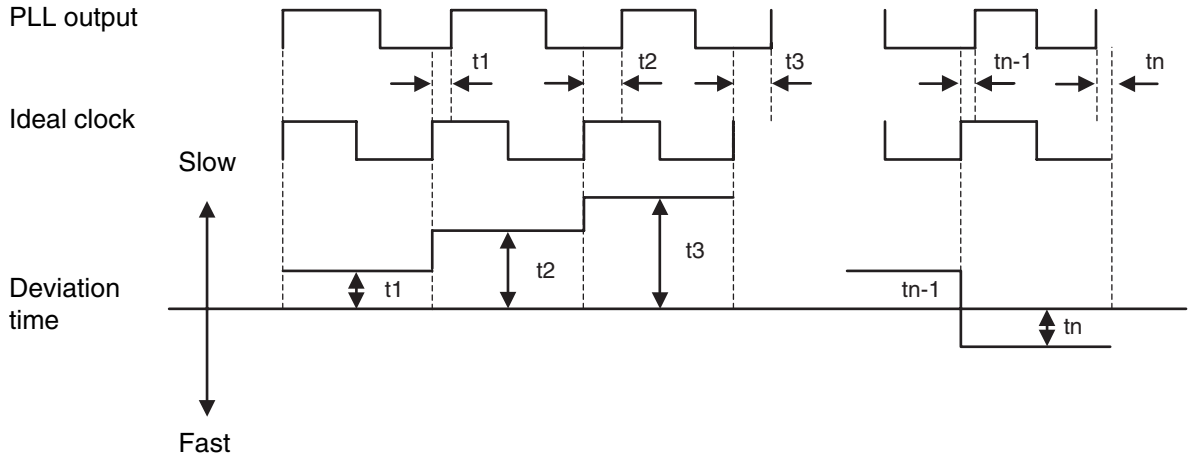
Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Frequency of source oscillation clock	F_C	X0, X1	—	—	4	—	MHz	
	Fca	X0A, X1A		—	32.768	—	kHz	
Source oscillation clock cycle time	t_{CYL}	X0, X1		—	250	—	ns	
Input clock pulse width	P_{WH}, P_{WL}	X0		100	—	—	ns	The duty ratio normally ranges from 40% to 60%.
Input clock rise/fall time	tcr, tcf	X0	—	—	—	5	ns	When external clock is used
Frequency of internal operating clock	F_{CP}	—		—	—	32	MHz	
Internal operating clock cycle time	t_{CP}	—	—	31.25	—	—	ns	
CAN PLL cycle jitter (When locked)	t_{PJ}	—	—	− 10	—	+ 10	ns	F_{CP} = 32 MHz (4 MHz, PLL multiplied by 8)

• X0/X1 Clock Timing



• CAN PLL cycle jitter

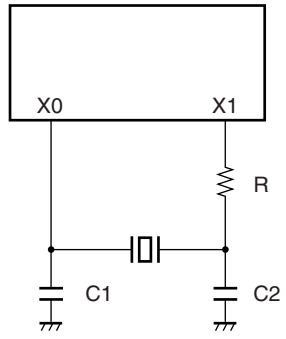
Deviation time from the ideal clock is assured per cycle out of 20, 000 cycles.



• Operations

Oscillation should be performed as described below :
[Source oscillation] : X0/X1 : 4 MHz, PLL : multiplied by 8, Internal frequency : 32 MHz
: X0A/X1A : 32 kHz, PLL : no multiplication, Internal frequency : 32 kHz
Note that the PLL oscillation stabilization wait time should be set to 500 µs or more.

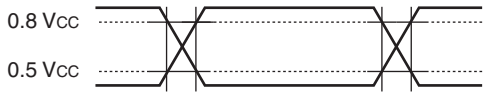
Sample oscillation circuit



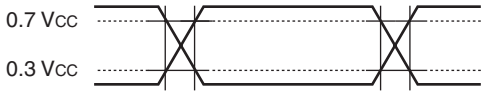
AC specifications are defined by the following measurement standard voltage values :

- Input signal wave form

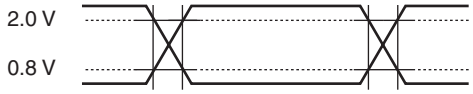
  Automotive input pin



  CMOS input pin

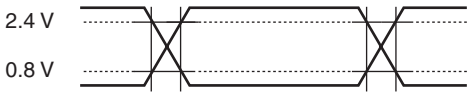


  TTL input pin



- Output signal wave form

  Output pin

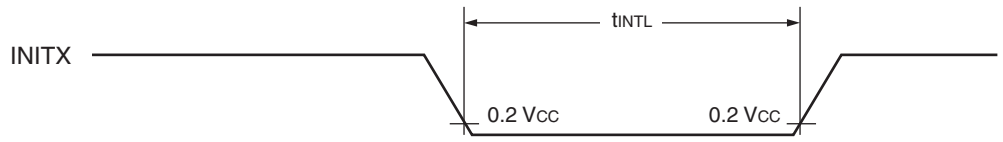


(2) Reset input

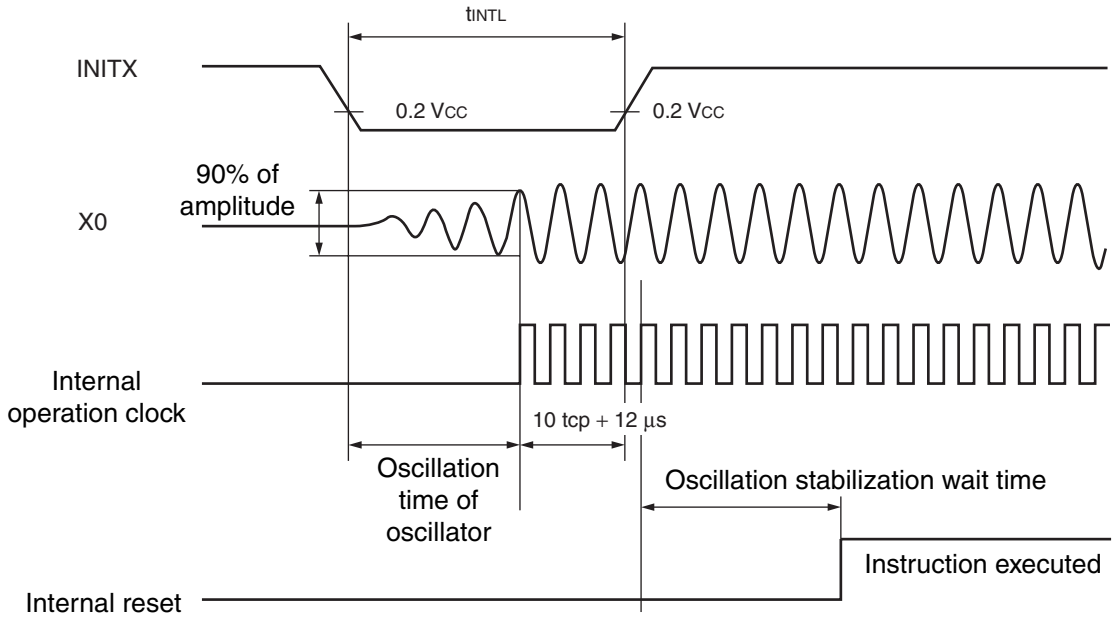
(T_A : − 40 °C to + 105 °C; Vcc = 5.0 V ±10%, V_{SS} = DV_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
INITX input time	t_{INTL}	INITX	—	500	—	ns	Under normal operation
				Oscillation time of oscillator* + 10 tcp + 12 µs	—	ms	In stop mode

* : The oscillation time of the oscillator refers to the time when the amplitude has reached 90%. The oscillation time of the crystal oscillator ranges from several ms to tens of ms. The oscillation time of the ceramic oscillator ranges from several hundreds to several ms, while that of the external clock is 0 ms.



• In stop mode

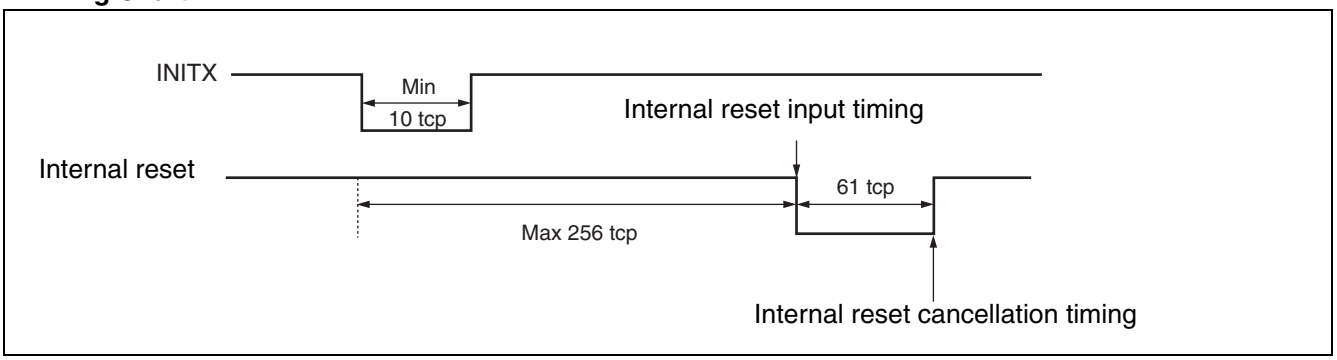


[External reset input specifications (INITX) and internal reset signal cancellation timing]

- When an external reset input is generated, a maximum of 256 tcp is designed to be spent until it reaches the internal reset signal to transmit all reset signals to the internal logic (Max 8 μs at 32 MHz) .
- The following chart shows how to set the timing for instruction execution start (start of application operation) after external reset input.

Time from external reset input to instruction start = Max 256 tcp + 61 tcp

• Timing Chart

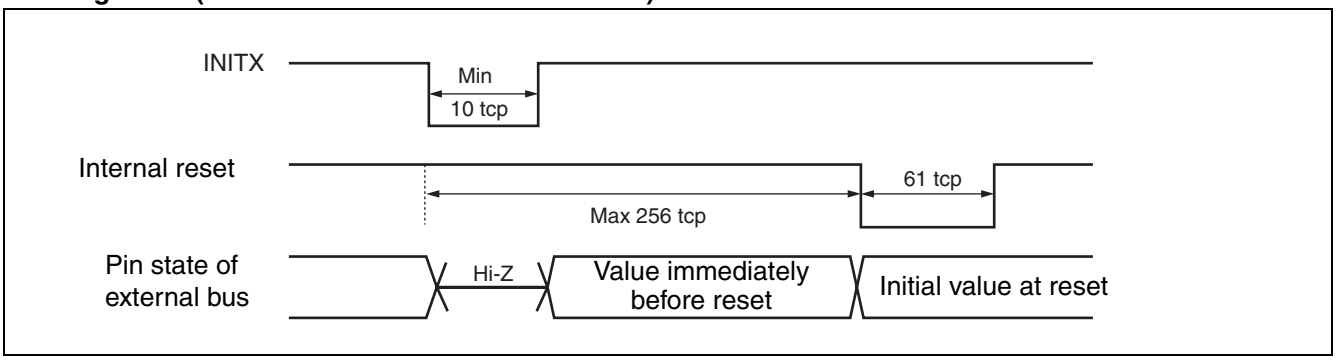


[Pin state in external bus mode]

In the external bus mode, it is not guaranteed to hold the RAM value upon external reset (INITX = “0”) input.

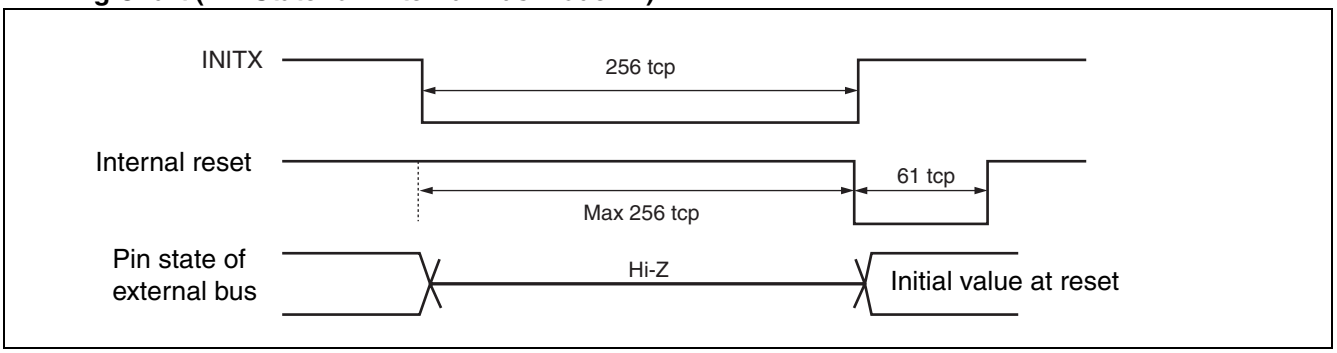
Beside that, the value of the internal bus is to be output to each pin during the time between the internal reset input and its cancellation.

• Timing Chart (Pin State for External Bus Mode : 1)



It can be avoided by the following external reset input to continue Hi-Z.

• **Timing Chart (Pin State for External Bus Mode : 2)**



(3) Power-on Conditions

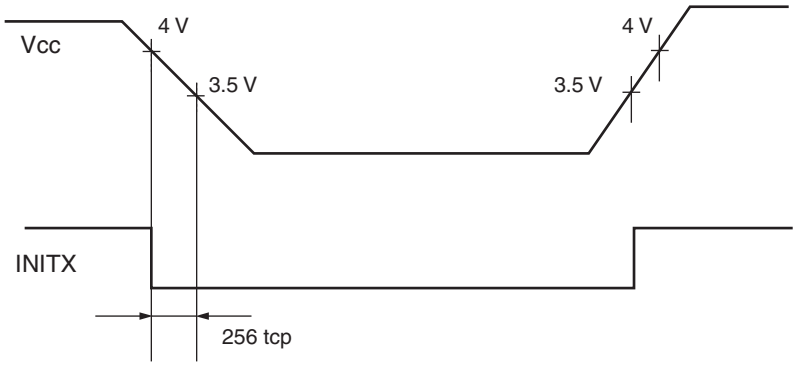
(T_A : − 40 °C to + 105 °C; V_{SS} = 0.0 V)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Power supply rising time	t_R	VCC	—	0.05	30	ms	
Power supply start voltage	V_{OFF}			—	0.2	V	
Power supply peak voltage	V_{ON}			2.7	—	V	
Power supply cut-off time	t_{OFF}			50	—	ms	Due to the repetitive operation

Power supply drop time, power supply voltages and external reset input to retain RAM data in MB91220/S

Satisfy the following reset input standard to retain the RAM data used in the single chip mode.

Vcc (V)	Voltage drop time	External reset input standard (INITX)
dropped 4.0 V → 3.5 V	Min 256 tcp	Min 256 tcp

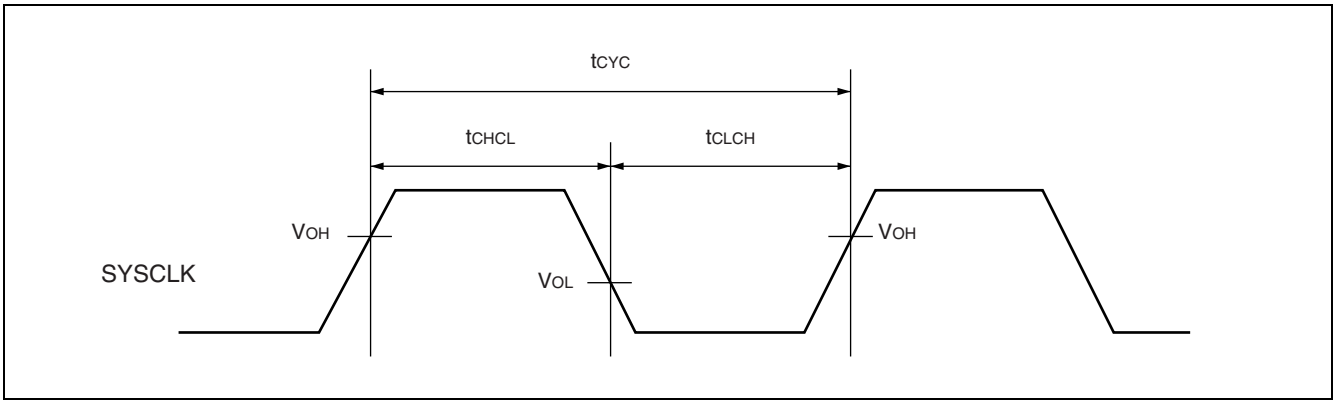


To retain RAM data, enter 256 tcp of INITX or more before dropping V_{CC} to 3.5 V or lower.

(4) Clock Output Timing

(V_{CC} = 4.5 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Cycle time	t_{CYC}	SYSCLK	—	t_{CPT}	—	ns	*1
SYSCLK↑→SYSCLK↓	t_{CHCL}	SYSCLK		t_{CYC} / 2 – 10	t_{CYC} / 2 + 10	ns	*2
SYSCLK↓→SYSCLK↑	t_{CLCH}	SYSCLK		t_{CYC} / 2 – 10	t_{CYC} / 2 + 10	ns	*3



*1 : t_{CYC} is the frequency of one clock cycle including the gear cycle.

*2 : The rating is under the conditions of “gear cycle × 1”.
When the gear cycle is set to 1/2, 1/4 or 1/8, use the formula below by entering 1/2, 1/4 or 1/8 in “n” respectively.

$$(1 / 2 \times 1 / n) \times t_{CYC} - 10$$

*3 : The rating is under the conditions of “gear cycle × 1”.

(5) Normal Bus Access : Read/Write Operation

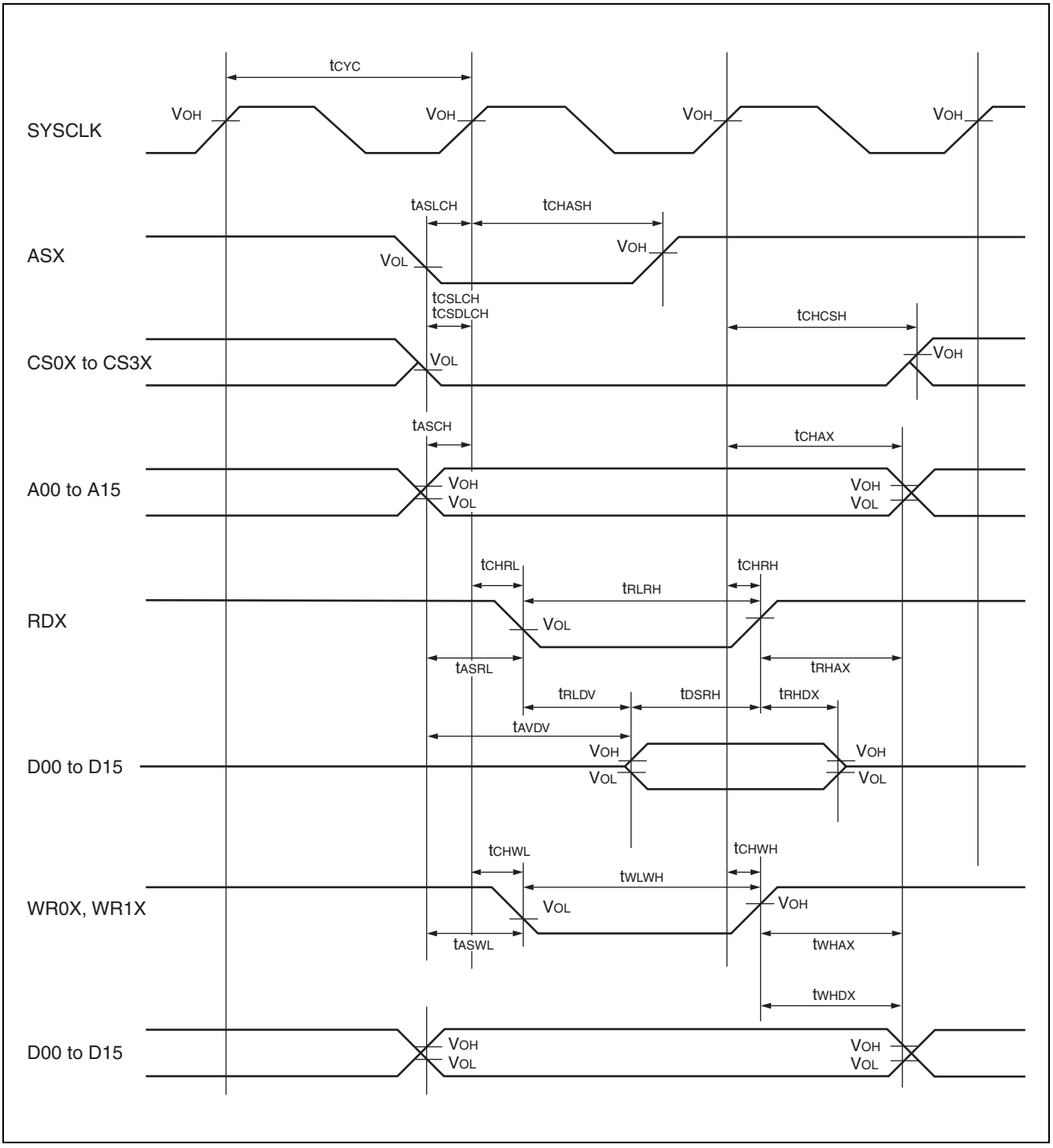
(V_{CC} = 4.0 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_A = 0 °C to + 70 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
CS0X to CS3X setup	t_{CSLCH}	SYSCLK CS0X to CS3X	AWRxL : W02 = 0	3	—	ns	
	t_{CSDLCH}		AWRxL : W02 = 0	–10	—	ns	
CS0X to CS3X hold	t_{CHCSH}			3	t_{CYC} / 2 + 30	ns	
Address setup	t_{ASCH}	SYSCLK A00 to A15		3	—	ns	
	t_{ASWL}	WR0X, WR1X A00 to A15		3	—	ns	
	t_{ASRL}	RDX A00 to A15		3	—	ns	
Address hold	t_{CHAX}	SYSCLK A00 to A15		3	t_{CYC} / 2 + 30	ns	
	t_{WHAX}	WR0X, WR1X A00 to A15		3	—	ns	
	t_{RHAX}	RDX A00 to A15		3	—	ns	
Valid address → valid data input time	t_{AVDV}	A00 to A15 D00 to D15		—	3 / 2 × t_{CYC} + 45	ns	*1, *2
WR0X, WR1X ↓ delay time	t_{CHWL}	SYSCLK WR0, WR1		—	10	ns	
WR0X, WR1X ↑delay time	t_{CHWH}			—	10	ns	
WR0X, WR1X minimum pulse width	t_{WLWH}	WR0X, WR1X		t_{CYC} – 10	—	ns	
Write data hold time	t_{WHDX}	WR0X, WR1X, D00 to D15		3	—	ns	
RDX ↓ delay time	t_{CHRL}	SYSCLK RDX		—	10	ns	
RDX ↑delay time	t_{CHRH}			—	10	ns	
RDX ↓ → valid data input time	t_{RLDV}	RDX D00 to D15		—	t_{CYC} – 30	ns	*1
Data setup → RDX ↑ time	t_{DSRH}			3	—	ns	
RDX ↑ → data hold time	t_{RHDX}			3	—	ns	
RDX minimum pulse width	t_{RLRH}	RDX		t_{CYC} – 10	—	ns	
ASX setup	t_{ASLCH}	SYSCLK ASX		3	—	ns	
ASX hold	t_{CHASH}			3	t_{CYC} / 2 + 25	ns	

*1 : If the bus is expanded by automatic wait insertion or RDY input, add time (t_{CYC} × the number of expanded cycles) to the rated value.

*2 : The rating is under the conditions of “gear cycle × 1”. When the gear cycle is set to 1/2 to 1/16, use the formula below by entering 1/2 to 1/16 in “n” respectively.

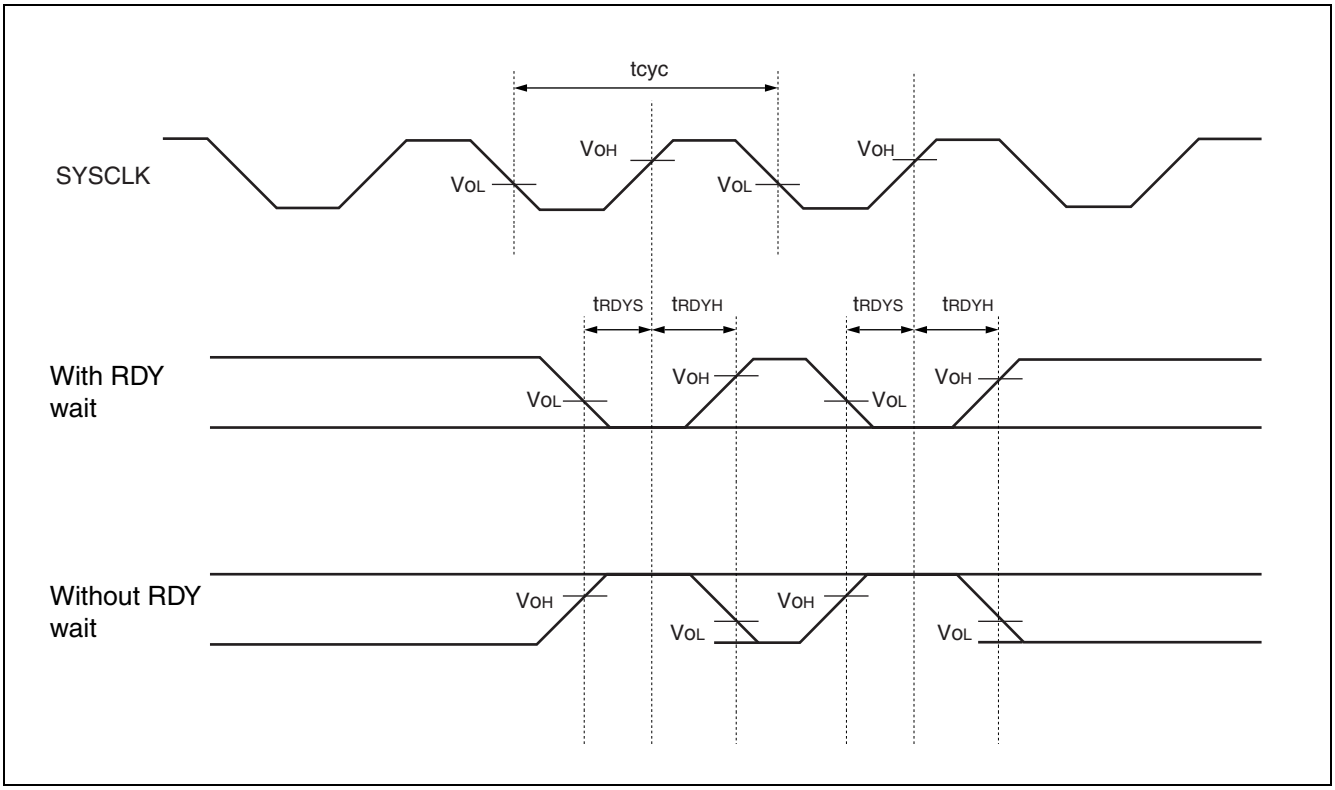
Formula : 3/ (2n) × t_{CYC} + 45



(6) Ready Input Timing

(V_{CC} = 4.5 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
RDY setup time →SYSCLK↓	t_{RDYS}	SYSCLK RDY	—	15	—	ns
SYSCLK↑→ RDY hold time	t_{RDYH}	SYSCLK RDY		0	—	ns



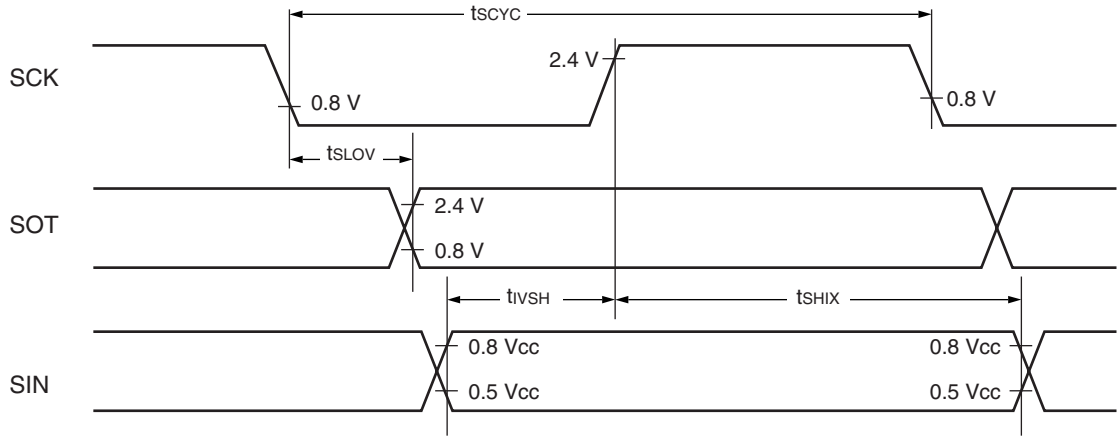
(7) UART Timing

(T_A : − 40 °C to + 105 °C; V_{CC} = 5.0 V ±10%, V_{SS} = AV_{SS} = 0.0 V)

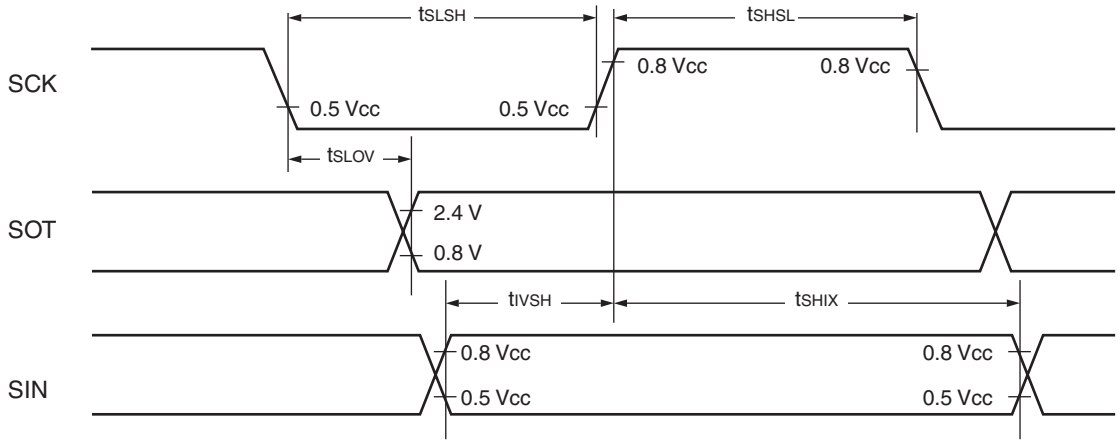
Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Serial clock Cycle time	t_{SCYC}	SCK0, SCK3 to SCK5	—	8 t_{CP}	—	ns	In internal shift clock mode, output pin; C_L = 80 pF+1 TTL
SCK↓→ SOT delay time	t_{SLOV}	SCK0, SCK3 to SCK5, SOT0, SOT3 to SOT5		− 80	+ 80	ns	
Valid SIN→ SCK↑	t_{IVSH}	SCK0, SCK3 to SCK5, SIN0, SIN3 to SIN5		100	—	ns	
SCK↑→ Valid SIN hold time	t_{SHIX}			60	—	ns	
Serial clock “H” pulse width	t_{SHSL}	SCK0, SCK3 to SCK5	—	4 t_{CP}	—	ns	In internal shift clock mode, output pin; C_L = 80 pF+1 TTL
Serial clock “L” pulse width	t_{SLSH}			4 t_{CP}	—	ns	
SCK↓→ SOT delay time	t_{SLOV}	SCK0, SCK3 to SCK5, SOT0, SOT3 to SOT5		—	150	ns	
Valid SIN→ SCK↑	t_{IVSH}	SCK0, SCK3 to SCK5, SIN0, SIN3 to SIN5		60	—	ns	
SCK↑→ Valid SIN hold time	t_{SHIX}			60	—	ns	

Notes : • The above ratings are the values for clock synchronous mode.
• C_L is a load capacitance connected to pins during testing.

• Internal Shift Clock Mode



• External Shift clock Mode

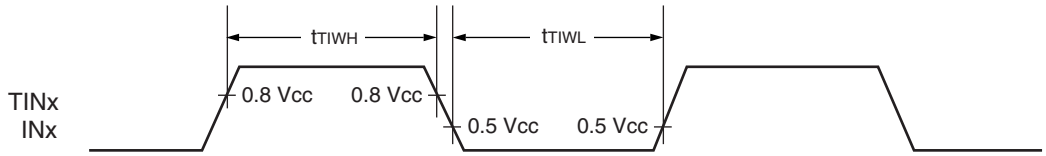


(8) Timer Input Timing

(T_A : − 40 °C to + 105 °C; V_{CC} = 5.0 V ±10%, V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Input pulse width	t_{TIWH} t_{TIWL}	TIN0 to TIN2, PWC0 IN0 to IN3	—	4 t_{CP}	—	ns

• Timer Input Timing

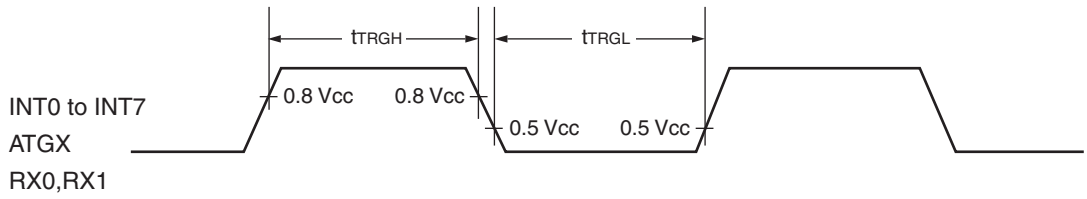


(9) Trigger input Timing

(T_A : − 40 °C to + 105 °C; V_{CC} = 5.0 V ±10%, V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TRGH}, t_{TRGL}	INT0 to INT7, ATGX, RX0, RX1	—	5 t_{CP}	—	ns	
				1	—	µs	At STOP mode

• Timer input timing



6. A/D Converter Electrical Characteristics

(1) Electrical Characteristics

(T_A : − 40 °C to + 105 °C; V_{CC} = AV_{CC} = 5.0 V ±10%, V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	—	—	—	—	10	bit	
Total error	—	—	—	—	±3.0	LSB	
Non-linearity error	—	—	—	—	±2.5	LSB	
Differential linearity error	—	—	—	—	±1.9	LSB	
Zero transition voltage	V_{OT}	AN0 to AN23	AV_{SS} − 1.5 LSB	AV_{SS} + 0.5 LSB	AV_{SS} + 2.5 LSB	V	1 LSB = (AVRH − AV_{SS}) / 1024
Full-scale transition voltage	V_{FST}	AN0 to AN23	AVRH − 3.5 LSB	AVRH − 1.5 LSB	AVRH + 0.5 LSB	V	
Sampling time	t_{SMP}	—	600	—	—	ns	AV_{CC} ≥ 4.5 V*1
			1200	—	—	ns	4.0 V ≤ AV_{CC} < 4.5 V*2
Compare time	t_{CMP}	—	990	—	—	ns	AV_{CC} ≥ 4.5 V*1
			1980	—	—	ns	4.0 V ≤ AV_{CC} < 4.5 V*2
A/D conversion time	t_{CNV}	—	3	—	—	µs	t_{SMP} + t_{CMP}
Analog port input current	I_{AIN}	AN0 to AN23	—	—	10	µA	AV_{CC} ≤ V_{AIN} ≤ AV_{SS}
Analog input voltage	V_{AIN}	AN0 to AN23	0	—	AVRH	V	
Standard voltage	AVR+	AVRH	4.0	—	AVcc	V	
Power supply current	I_A	AVCC	—	2.4	4.7	mA	
	I_{AH}		—	—	5	µA	*3
Standard voltage supply current	I_R	AVRH	—	500	900	µA	V_{AVRH} = 5.0 V
	I_{RH}	AVRH	—	—	5	µA	*3
Variation between channels	—	AN0 to AN23	—	—	5	LSB	

*1 : Assume that the output impedance of the external analog signal is 2.74 kΩ or less. If the output impedance is high, the sampling time is longer than the standard value (refer to note) . For actual use, set t_{CNV} ≤ t_{SMP} + t_{CMP}.

*2 : Assume that the output impedance of the external analog signal is 0.7 kΩ or less. If the output impedance is high, the sampling time is longer than the standard value (refer to note) . For actual use, set t_{CNV} ≤ t_{SMP} + t_{CMP}.

*3 : This defines the power supply current when the A/D converter is not in operation and the CPU is stopped (at V_{CC} = AV_{CC} = AVRH = 5.0 V) .

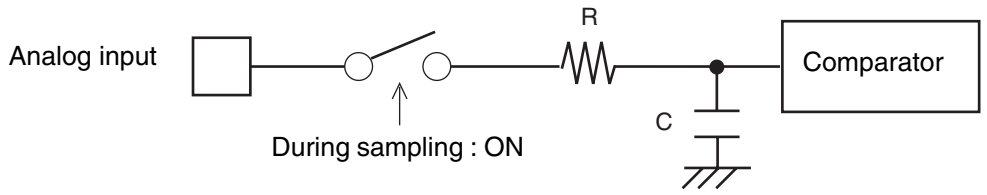
(Continued)

(Continued)

Note : The external impedance of the analog input and its sampling time
A/D converter with sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the internal sampling and hold capacitor is insufficient. Therefore, it adversely affects A/D conversion precision

.

• Analog input circuit model



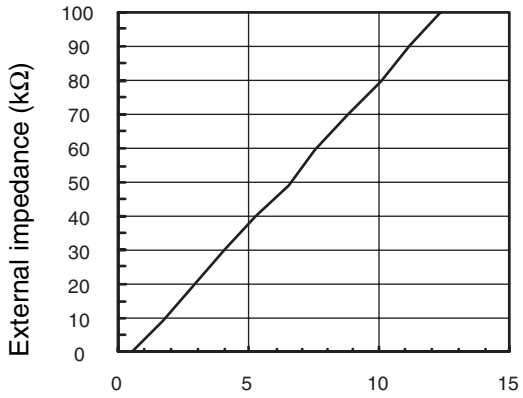
	R	C
Note : The values are reference values.	3.95 kΩ (max)	17 pF (max)

To satisfy the A/D conversion precision standard, adjust the register value and operating frequency, or decrease the external impedance in accordance with the relationship between the external impedance and minimum sampling time, in order to make the sampling time longer than the minimum value.

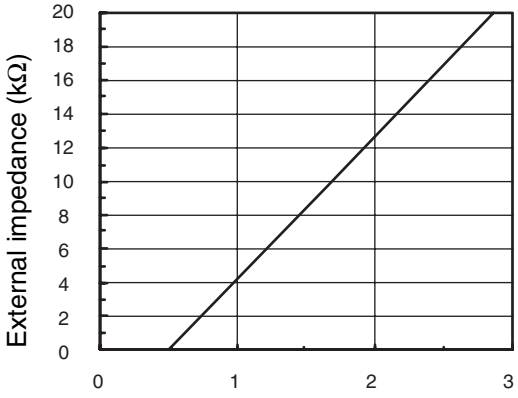
- **The relationship between the external impedance and minimum sampling time**

- At 4.5 V ≤ AV_{CC} ≤ 5.5 V

[External impedance = 0 kΩ to 100 kΩ]

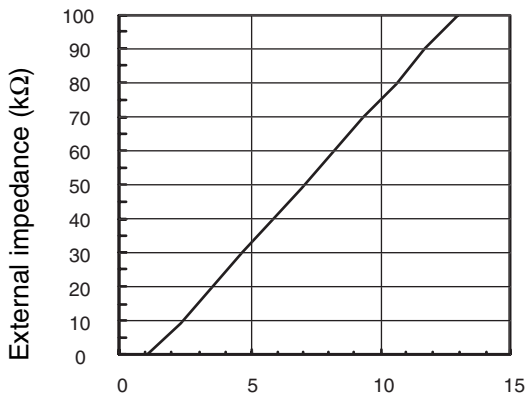


[External impedance = 0 kΩ to 20 kΩ]

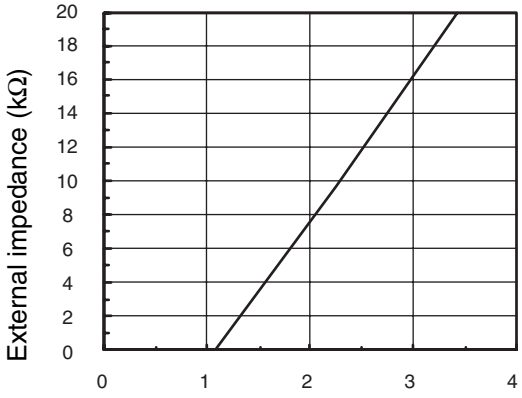


- At 4.0 V ≤ AV_{CC} < 4.5 V

[External impedance = 0 kΩ to 100 kΩ]



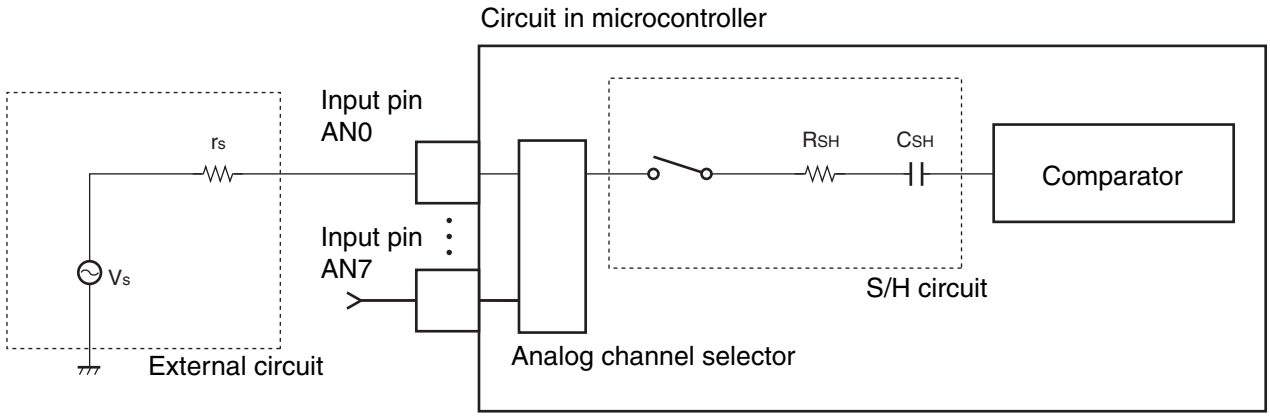
[External impedance = 0 kΩ to 20 kΩ]



- If the sampling time is not sufficient, connect a capacitor of about 0.1 µF to the analog input pin.

- Measure against noise for reference power supply (AVRH pin)
  It is recommended that a bypass capacitor of several µF be input to the reference power supply (AVRH) .
- About errors
  |AVRH − AV_{SS}| becomes smaller, values of relative errors grow larger.
- Others
  When placing a DC blocking capacitor between the external circuit and input pin,set the capacitance value by multiplying C_{SH} and several thousands as a guideline in order to minimize the impact from dividing voltage capacitance with C_{SH}.

• Analog Input Equivalent Circuit



<Recommended parameter values for each element>

r_S = 5 kΩ or less

R_{SH} = approx. 2.5 kΩ

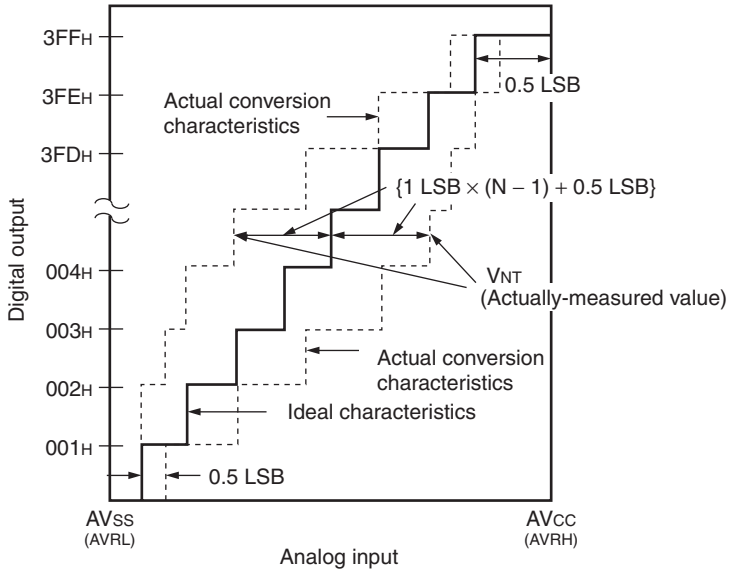
C_{SH} = approx. 10 pF

Note : These element parameters should be regarded as tentative values used only for design purposes. They do not guarantee the operation.

(2) Term Definitions

- Resolution
  Level of analog variation that can be distinguished by the A/D converter.
  When the number of bits is 10, the analog voltage can be resolved into $2^{10} = 1024$.
- Total error
  Difference between actual and theoretical values, which is a total value derived from an offset error, gain error, non-linearity error and noise.
- Linearity error
  Deviation between the value along a straight line connecting the zero transition point
  (“00 0000 0000”←→“00 0000 0001”) of a device and the full-scale transition point
  (“11 1111 1110”←→“11 1111 1111”) compared with the actual conversion values obtained.
- Differential linearity error
  Deviation of input voltage, which is required for changing output code by1 LSB, from an ideal value.

Total error



$$\text{Total error of digital output “N”} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + 0.5\ \text{LSB}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$1\ \text{LSB (Ideal value)} = \frac{AV_{CC} - AV_{SS}}{1024}\ [\text{V}]$$

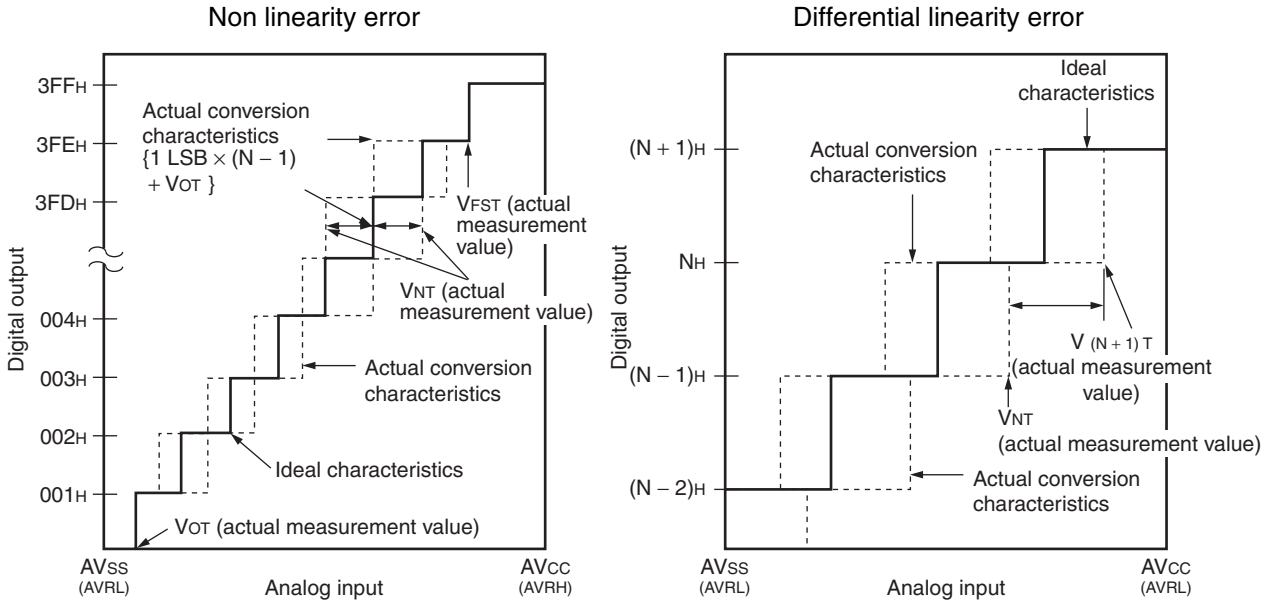
V_{OT} (Ideal value) $= AV_{SS} + 0.5$ LSB [V]

V_{FST} (Ideal value) $= AV_{CC} - 1.5$ LSB [V]

V_{NT} : A voltage at which digital output transits from $(N - 1)_H$ to N_H.

(Continued)

(Continued)



$$\text{Non linearity error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + V_{OT}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$\text{Differential linearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1\ \text{LSB}\ [\text{LSB}]$$

$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ [\text{V}]$$

N : A/D converter digital output value
V_{OT} : Voltage at which digital output transits from “000_H” to “001_H.”
V_{FST} : Voltage at which digital output transits from “$3FE_H$” to “$3FF_H$.”

7. Electrical Characteristics for the D/A Converter

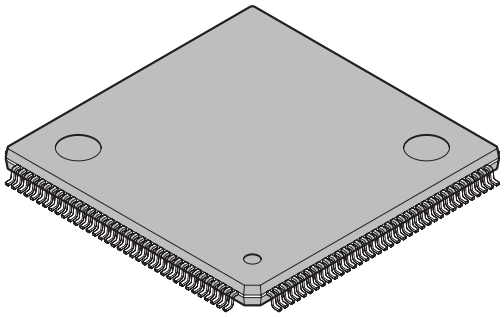
(T_A : − 40 °C to + 105 °C; V_{CC} = AV_{CC} = 5.0 V ±10%, V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	—	—	—	—	8	bit	
Differential linearity error	—	—	—	—	±3	LSB	
Conversion time	—	—	—	0.45	—	µs	At load capacitance 20 pF
	—	—	—	2.00	—	µs	At load capacitance 100 pF
Reference power supply current	I_{DVR}	AVCC	—	162	920	µA	T_A = + 25 °C
	I_{DVRS}	AVCC	—	—	0.1	µA	At power down
Analog output impedance	—	—	2.0	3.0	3.9	kΩ	

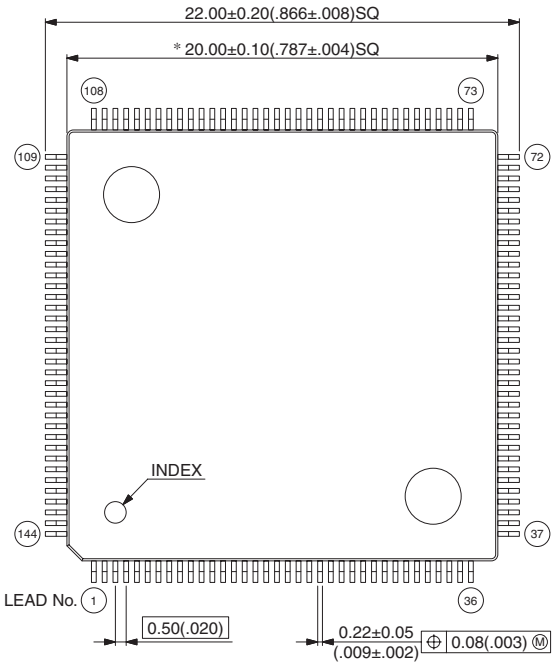
■ ORDERING INFORMATION

Part number	Package	Remarks
MB91V220ACR-ES	401-pin ceramic PGA (PGA-401C-A02)	Evaluation product
MB91F223PFV-GSE1	144-pin plastic LQFP (FPT-144P-M08)	Sub clock support
MB91F223SPFV-GSE1	144-pin plastic LQFP (FPT-144P-M08)	Sub clock not yet support

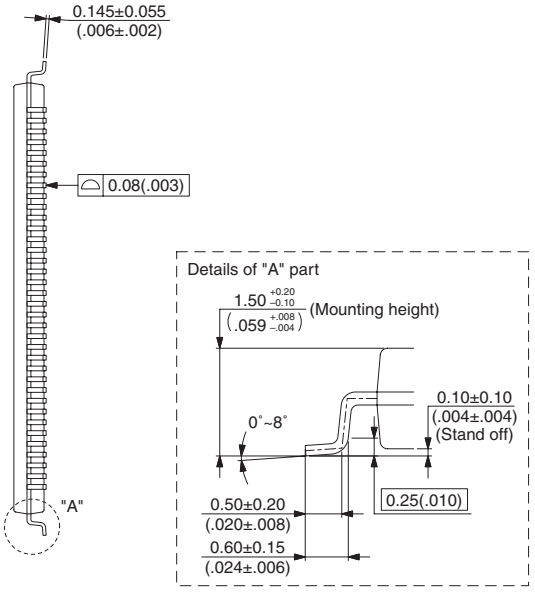
■ PACKAGE DIMENSION

144-pin plastic LQFP		
	Lead pitch	0.50 mm
	Package width × package length	20.0 × 20.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	1.20g
(FPT-144P-M08)	Code (Reference)	P-LFQFP144-20×20-0.50

144-pin plastic LQFP
(FPT-144P-M08)



Note 1) *:Values do not include resin protrusion.
Resin protrusion is +0.25(.010)Max(each side).
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please confirm the latest Package dimension by following URL.
http://edevice.fujitsu.com/fj/DATASHEET/ef-ovpklv.html

The information for microcontroller supports is shown in the following homepage.
http://www.fujitsu.com/global/services/microelectronics/product/micom/support/index.html

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